03M13B20

VISUAL

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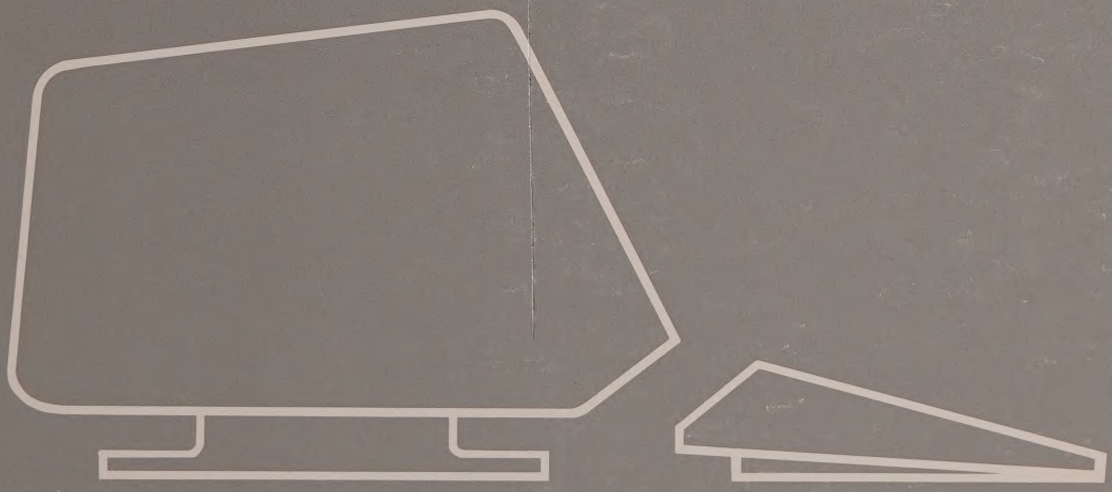
MAINTENANCE MANUAL

VISUAL 500/550



WARNING

This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instruction manual may cause interference to communications. It has been tested and found to comply with the limits for Class A computing devices pursuant to Subpart J of Part 15 of FCC rules which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference, in which case the user, at his own expense will be required to take whatever measures may be required to correct the interference.

VISUAL TECHNOLOGY INCORPORATED, 540 MAIN STREET, TEWKSBURY, MA 01876

V500/550

VIDEO DISPLAY TERMINAL
MAINTENANCE MANUAL

January 1983

SAFETY WARNING

Hazardous voltages 115, 220 VAC and 15 KV DC are present when the terminal is on, and may remain after power is removed. Use caution when working on internal circuits, and do not work alone.

When handling the cathode ray tube caution is required as the internal phosphor is toxic. Safety goggles and gloves must be used whenever the CRT tube is handled. If the tube should break, and skin or eyes are exposed to the phosphor, rinse the affected area with cold water and consult a physician.

This terminal is supplied with a cord set which includes a safety ground. Do not use this terminal with an ungrounded outlet, missing ground pin, or use any adaptor which will defeat the safety ground.

Insure that power is turned off before connecting or disconnecting the keyboard cable.

This manual is published and distributed by Visual Technology Inc. Every effort has been exercised to insure its accuracy and completeness. The contents are subject to change without notice and this manual may not reflect the latest changes. Consult the sales department for latest changes.

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1. ARCHITECTURE

The Visual 500/550 is a microprocessor (Z80) based terminal composed of SSI, MSI and LSI logic elements. The communications/keyboard receiver, the printer interface receiver, and the video refresh are interrupt driven.

Program memory consists of a maximum of 32K bytes of either PROM or ROM organized as 4-2Kx8 devices or 4-8Kx8 devices.

RAM memory is organized into 3 groups. Alpha memory, 4Kx8, is organized in two 2Kx8 groups. One for data and the other for attributes. This memory is connected to the video address bus rather than the Z80 address bus. The second memory group is the graphics RAM. 32Kx16, providing a full bit map and again is not connected to the Z80 address bus, but rather to the graphics video address bus. The third RAM area, and the only one connected to the Z80 address bus, is a 2Kx8 scratch pad RAM.

A battery backed-up CMOS RAM (1Kx4) is provided to store SET-UP parameters.

All timing other than data rates, is derived from a crystal oscillator. Each frame is refreshed at 30Hz rate in an interlaced manner. Data Rate timing is derived from a second crystal oscillator to insure accurate encoding and decoding of serial data.

Each character is created in a 9x15 dot matrix field in which upper case characters are 7x9 and lower case characters 7x11.

While 80 characters are displayed on each line, the timing allows 100 character times per line horizontally, resulting in the display being centered within the raster.

Vertically, each frame consists of 34 lines with each line being 15 raster lines high. While this requires 510 raster lines, the Visual 500/550 generates 645 lines to center the display vertically. The following calculations describe the above relationship:

80 Character Mode

(30 Hz) x (9 dots/character) x (100 characters/line) x (645 lines/frame) x (2) = 34.65 MHz.

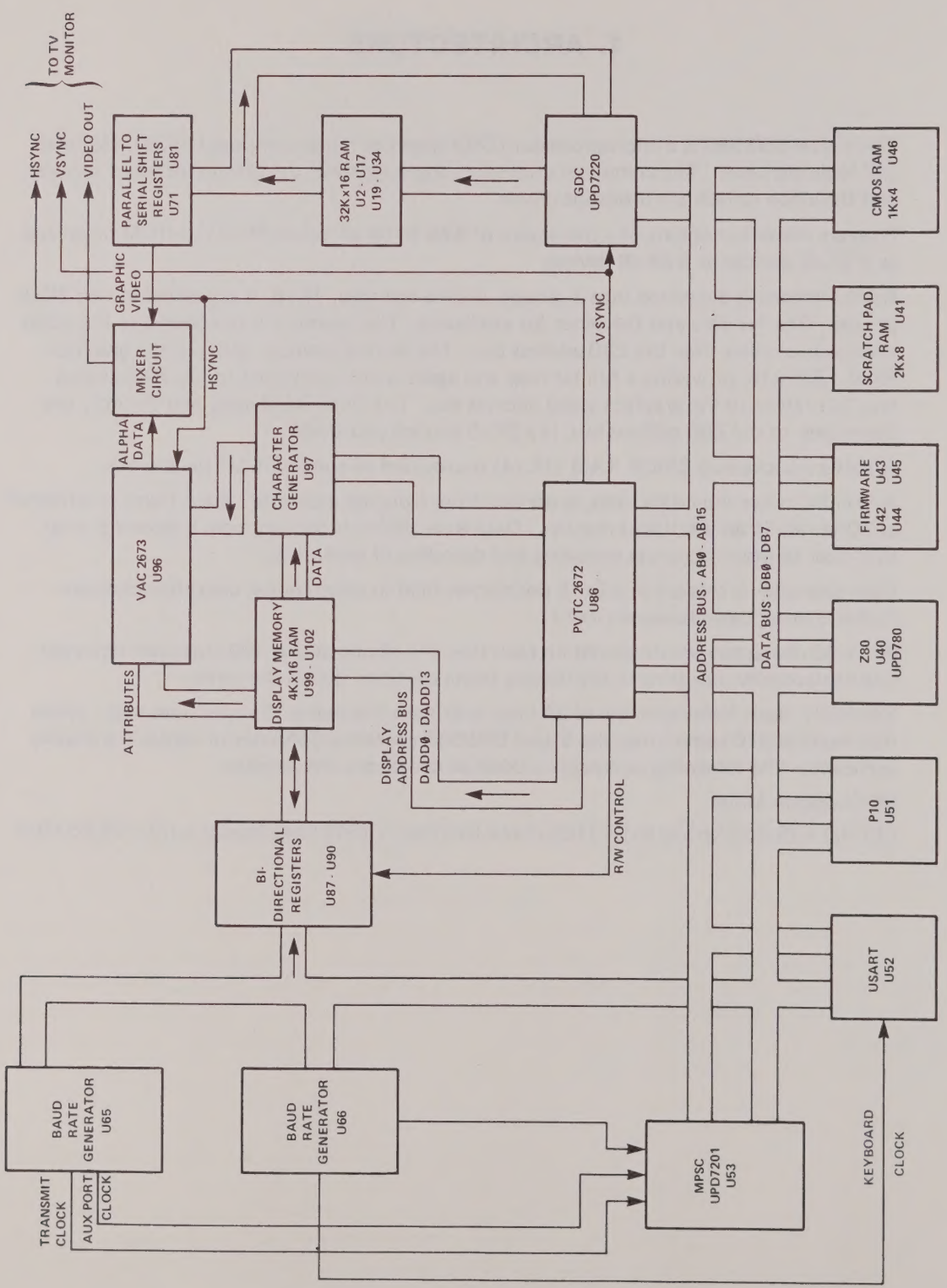

TO TV MONITOR
HSYNC
VSYNC
VIDEO OUT
PARALLEL TO SERIAL SHIFT REGISTERS U71 U81
32Kx16 RAM U2 - U17 U19 - U34
GDC UPD7220
CMOS RAM 1Kx4 U46
GRAPHIC VIDEO
MIXER CIRCUIT
HSYNC
V SYNC
SCRATCH PAD RAM 2Kx8 U41
ALPHA DATA
CHARACTER GENERATOR U97
VAC 2673 U96
PVTC 2672 U86
FIRMWARE U42 U43 U44 U45
DATA
DISPLAY MEMORY 4Kx16 RAM U99 - U102
ADDRESS BUS - AB0 - AB15
DATA BUS - DB0 - DB7
Z80 U40 UPD780
ATTRIBUTES
DISPLAY ADDRESS BUS
DADD0 - DADD13
P10 U51
BI-DIRECTIONAL REGISTERS U87 - U90
R/W CONTROL
USART U52
BAUD RATE GENERATOR U65
BAUD RATE GENERATOR U66
MPSC UPD7201 U53
TRANSMIT CLOCK
AUX PORT CLOCK
KEYBOARD CLOCK

Figure 1

2. THEORY OF OPERATION

The Visual 500/550 electronics are located on 3 circuit boards: the TV electronics, Logic PCB, and power supply. The Logic PCB is organized in columns of IC's designated by a U number. These IC's are numbered sequentially starting in the top left corner and proceeding from top to bottom and from left to right. The schematic diagrams contained in this manual utilize this numbering system which eliminates the need for a parts location diagram.

2.1 MASTER TIMING

Sheet 5 of the schematics contains the crystal oscillator, operating at 34.65 MHz, which provides all timing for the terminal. This clock is divided by 2 to form the Dot Clock (DCLK) at 17.325 MHz. U74 is used to divide DCLK by 8 to generate PCLOCK. PLOCK, at 2.165 MHz, is used by the Z80 microprocessor. U96 the 2673 chip on sheet 4, divides DCLK (pin 32) by 9 (9 dots per character horizontally, 7 active and 2 intercharacter space) to form the character clock (CCLK), on pin 36, at 1.925 MHz.

2.2 DATA RATE TIMING

Sheet 5 of the schematics contains the data rate crystal oscillator. Y1 operating at 1.8432 MHz through U83 and U63 to DATACLK and DATACLK, is used by the baud rate generators U66 and U65 on sheet 4 to generate the transmit, receive, printer and keyboard serial clocks.

2.3 MICROPROCESSOR OPERATION

On sheet 1 of the schematics, the microprocessor (Z80) is shown as chip U40. The Z80 generates 16 bits of address (AB0 - AB15) which are decoded to form memory and device addresses. The Video Memory, used for display refresh, is not addressed directly by the Z80 and, as such, does not use the Z80 address bus. The video memory is addressed by the 267X video chip set and is accessible by the data bus only during horizontal blanking time and only through a hand-shaking procedure with the 267X chip set. Because of this arrangement the Z80 does not use a DMA cycle, and operates in the I/O mode only.

Maskable and non-maskable interrupts are serviced in mode 1 by generating a CALL to one of two program locations. Combined interrupt (CINT) is generated by the keyboard and the printer, when installed, and makes use of the Z80's maskable interrupt input causing a CALL to location 0038. The non-maskable interrupt input of the Z80 is used by the video (VIDIPT). The video interrupt occurring for each character line (980ms.) and for each frame (16.66ms.) causes a CALL to location 0066.

2.4 PROGRAM MEMORY

The Visual 500/550 has been designed to allow the use of 2Kx8, 4Kx8 or 8Kx8 EPROMS. Locations U42, U43, U44 and U45 are capable of receiving 24 or 28 pin sockets. 24 pin sockets are used by 2716 and 2732 PROMS, while 2764 PROMS require 28 pin sockets. If 28 pin sockets are installed and 2716 of 2732 PROMS are used, it is necessary to install these PROMS so that they use the right most set of pins (pins 1, 2, 27 28 of the 28 pin socket are vacant when a 24 pin device is installed).

On sheet 1 of the schematics U37 and U38 decodes the select for each of the PROMS (ROMØ, ROM1, ROM2, and ROM3). In addition U38 is used to decode the address for the CMOS non-volatile RAM and the RAM used for memory. Note that the CMOS RAM (CRAMS) uses the same address as ROM3. This is possible because the program, through the PIO, selects either ROM3 or CRAMS with the signal ACRAM.

Figure 2-1 illustrates the relationship between PROM size, address and jumper configuration. See Figure 2-4 for jumper locations.

SIZE	TYPE	ROMØ U42	ROM1 U43	ROM2 U44	ROM3 U45	JUMPERS					
						W1	W2	W3	W4	W5	W6
2Kx8	2716	0000-07FF	0800-0FFF	1000-17FF	1800-1FFF	0	1	1	0	0	1
4Kx8	2732	0000-0FFF	2000-2FFF	1000-1FFF	3000-3FFF	1	1	0	0	1	0
8Kx8	2764	0000-1FFF	2000-3FFF	4000-5FFF	6000-7FFF	1	0	0	1	1	0

1 = INSTALL 0 = OMIT

Figure 2-1. PROM Addressing

Note that addressing is in sequential order for 16K and 64K PROMS but not for 32K. In ascending address order the PROM locations are: 16K and 64K – U42, U43, U44, U45, and for 32K – U42, U44, U43, U45. Visual's PROM labels automatically compensate for this order change by indicating the location into which each PROM is to be installed.

2.5 CMOS MEMORY

The CMOS memory, U46, provides for non-volatile storage of setup parameters. On sheet 2 of the schematics the CMOS RAM is shown together with the 3.4 volt lithium battery and diodes CR 7 and CR 8. When the terminal is powered on, 5 volts, through diode CR 8, supplies power to the RAM allowing Read and Write operations. When power is disconnected the RAM contents are maintained by the lithium battery and diode CR 7. Resistor R12 together with the transistors shown on sheet 1 which generate CRAMS insure that the CMOS RAM select input, CRAMS, is in a high impedance state when power is turned off.

No charging circuit for the battery is provided as minimal current is drawn, and the life expectancy of the battery approximates shelf life.

Because only 3 of the 5 high order address bits are used at any time to decode the ROM and CRAMS functions, each select will be repeated as addresses increase. CRAMS will be 1800 to 1AFF for 16K PROMS, or 3000 to 33FF for 32K, or 7000 to 73FF for 64K PROMS. In fact, regardless of PROM size and Jumpers installed, the CMOS RAM can be addressed at 7000-73FF, which is the way the firmware operates.

2.6 I/O BUS RAM

I/O bus RAM is required to provide a receive FIFO, transmit FIFO, Stack and scratchpad. U41, sheet 2 is utilized for this purpose. U41 is a 2Kx8 static RAM located at addresses 8000 to 87FF.

2.7 DISPLAY MEMORY

V500/550 has two display memories, alpha/numeric and graphic, which allows simultaneous display of alpha numeric and graphic data. The alpha/numeric memory consists of a pair of 2Kx8 static RAMS. One for data and a 2Kx8 static RAM for attributes. These RAMS are shown on schematic sheet 6. Note that the address bits for each of these devices is DADDØ rather than the Z80 address bus ADBØ.

Alpha/numeric data is loaded into and out of display memory through the use of an interrupt with a command to the 2672 programmable video timing controller (PVTC). When a character is written into the display RAM the Z80 stores the character in the write latch, U87 on sheet 6 together with any attribute associated with that character in U89 using SVDWR and SVAWR (Select Video Data and Attribute Write). The Z80 then issues a write command to the PVTC using the PVTC command register. At the next horizontal blanking interval, the PVTC enables the output drivers of the write latch and writes the data into the RAM by generating the Video Write signal VWR. A ready bit is available in the PVTC status register for I/O testing and an interrupt mask bit for ready is also available within the PVTC. On reading data from the video memory the process is similar. The Z80 issues a read command to the PVTC which will strobe the character into the read buffers, U88 and U90, at the next horizontal blanking interval using the Video Buffer Read signal (VBWR). Upon determining that the PVTC is ready by interrupt or status read, the Z80 places the contents of the read buffer onto the data bus by issuing the Select Video Read signal (SVDRD and SVARD). Because the data bus is only eight bits wide, reading and writing data and attributes to display memory require two bus operations in each direction. SVAWR and SVDWR select attribute of data write operations while SVARD and SVDRD select attribute or data read operations. These are decoded by the device address decoder on sheet 1 and are disucssed further in Section 2.8.

The graphic display memory has 32 uPD416 dynamic, 16Kx1 RAMS, arranged as a 32Kx16 plane. These RAMS are shown on sheet 9 of the schematics.

Graphic data is loaded into and out of the graphic memory by the Z80 issuing read and write commands through device decoder U62 and U61, sheet 1, which selects the Graphic Display Control (GDC) by use of Select Graphic Display Control Write (SGDCW) or Select Graphic Display Control Read (SGDCR). When SGDCW is issued to the Graphic Display Control, U39, on sheet 7. The GDC then generates a DBIN (Read Data to Display Memory Bus). DBIN, through flop U60 sheet 8 and combined with 2XWCLK through gate U82 sheet, issues a GMWR (Graphic Memory WRite) which enables pin 3 of graphic memory (sheet 9) U2 through U17 and U19 through U34. Then graphic data (ADØ – AD15) is written into graphic memory. When a SGDCR is issued by the Z80, the Graphic Display Control will issue an ORAS (read data out of memory). The ORAS combined with 8XWCLOCK through U48 sheet 8, generates a RAS (Row Address Strobe) first which enables RAMS U2 through U17 and U19 through U34. Then MUX is generated switching the address bits to the RAMS. When MUX is high the low order bits, ADØ through AD6 through multiplexer U18 and when MUX is low the high order bits AD7 – AD13 through the multiplexer U1. ACAS (Column Address Strobe) is generated next by U48, which is a combination of ACAS and 8XWCLK and is gated with the higher address bits (Case 1 and Case 2). If this is a valid memory address the RAMS are enabled on pin 15. Case 1 is a memory address between 0000 and 3FFF, while Case 2 is a valid address between 4000 and 7FFF. Case 1 enables RAMS U2 through U17, while Case 2 enables RAMS U19 through U34.

2.8 DEVICE ADDRESSING

On sheet 1 of the schematics, chips U62 and U77 decode all of devices addresses used throughout the terminal. Devices like the PIO, PVTC and USART use more than one address, as an example, the PVTC uses eight addresses. Each device is therefore assigned a block of 16 addresses as this provides more than enough capability and simplifies the decoding. Figure 2-2 shows the address assignments. Note that chip U77 has write (WR) as one of its inputs. This provides both a unique device address for 7Ø write and 7Ø read as well as 71 read and 71 write.

ADDRESS	MNEMONIC	FUNCTION
ØØ-ØF	Not Used	
1Ø-1F	SBRGØ	Strobe for communications and keyboard Baud Rate Generator
2Ø-2F	SPIO	Select PIO 2Ø = Port A, 21 = Port B, 22 = Port C, 23 = Control
3Ø-3F	SPUSART	Select Printer USART 3Ø = Data, 31 = Control Word
4Ø-4F	SMPSC	Select Multi-Protocol Serial Controller 7201 Communications Port and Keyboard Port
5Ø-5F	SBRG1	Strobe Baud Rate Generator (Printer Speed and Transmit Speed)
6Ø-6F	SVTAC	Select PVTC
7Ø WRITE	SVDWR	Select Video Data Write
7Ø READ	SVDRD	Select Video Data Read
71 WRITE	SVAWR	Select Video Attribute Write
71 READ	SVARD	Select Video Attribute Read

Figure 2-2. Device Addresses

2.8.1 PIO

The parallel input/output chip (PIO), U 51, is located on schematic sheet 1. Within the Visual 500/550, the PIO is programmed so that ports A and B operate in the output mode while port C is configured in the input mode. Five bits of port A (BRDØ-BRD4) provide 32 steps of video brightness. These five bits drive a ladder network on sheet 6 which controls the DC video level sent to the monitor PCB. One bit of port A (PREV) is used as the selection for Page Reverse Video or normal video. One bit of port A (BLINKF) provides the blink frequency for the video chip set. Blink occurs at a rate of .38 Hz and is program determined. The last bit of port A, ACRAM, selects the enable of the CMOS RAM or ROM3 when the appropriate memory address is generated.

Port B provides signals which are used to control communications functions. RDE (Receive Data Enable) allows external received data to be received. During functions such as transmit

in block mode, RDE inhibits the receiver. LDE (Local Data Enable) establishes a local copy function by allowing transmitted data into the receiver such as during conversation mode while in local. ACTS (Allow Clear-to-Send) permits CTS to be received, however, it forces the internal CTS during local operations and during current loop operation and allows the communications transmitter to function. TXE (Transmit Data Enable) allows transmit data to the RS 232 and current loop drivers, and inhibits data from these drivers while the terminal is switched to local.

All of these signals are used on schematic sheet 3. EGVID (Enable Graphics Video) allows the graphic data to be displayed on the screen. The last Port B signal, SYNC, is used to select external modem generated clocks in synchronous mode or internal generated communications clock asynchronous mode. U52 on sheet 2 is used for this selection, and is discussed further in Section 2.8.3. At present the 500/550 firmware does not support synchronous communications.

Port C operates in the input mode and allows the Z80 to test current status of data set ready (DSR), printer present (PPRES), printer interrupt (PIPT) and video interrupt (VIDIPT). Odd/Even Field (ODEVFL) senses the odd or even frame being refreshed.

2.8.2 Baud Rate Generator

On sheet 4 of the schematics, two baud rate generators are shown in location U65 and U66. Data via the data bus is strobed into the baud rate generators in two nibbles. U66 DBØ-DB3 select the receive rate (RXCLK) and DB4-DB7 set the keyboard rate (KBCLK) fixed by firmware at 600 Baud. U65 DBØ-DB3 select the transmit data (TXCLK) and DB4-DB7 select the printer rate (PRCLK). In all cases the data rate selected is a clock which has a rate 16 times the Baud rate selected. Detailed specifications on the baud rate generators is located in Section 5.

2.8.3 Rate Selector

On sheet 1 of the schematics, the multiplexer U54 is used to select which clock will be used for the communications transmit and receive. Pin 1 controls the selection such that in synchronous mode the transmit clock used (XMTCK) will always be the modem supplied clock (TXT). In like manner, the receiver clock (RECCK) will be the received clock (RXT) in synchronous mode.

In asynchronous mode, the transmitter will always use the baud rate generated transmit clock (TXCLK) regardless of the presence or absence of the printer option. The receiver, however, uses the transmit clock (TXCLK) when the printer option is not present, and uses the receive clock (RXCLK) when the printer option is present, allowing split baud rates. The V500/550 is normally supplied with the printer option installed.

In asynchronous mode receive and transmit clocks operate at 16 times the baud rate selected, while in synchronous mode they operate at 1 times the rate.

2.8.4 MPSC

The multi-protocol serial controller (MPSC) is a dual channel serial controller. Shown on sheet 4 as U53, it is used as the serial transmitter and receiver for the main communications port and as a serial transmitter and receiver for the keyboard. The communications channel

operating at whatever rate the baud rate generators select also provides drivers and receivers for the modem control lines such as Request to Send (RTS). Carrier Detect (DCD). Data Terminal Ready (DTR), Clear to Send (CTS), Secondary Channel Request to Send (SCRTS) and Secondary Channel Carrier Detect (SCCD).

2.8.5 Keyboard Logic

The keyboard on the V500/550 operates in a serial fashion, over a telephone type modular cable. The V500/550 issues scanning commands and bell commands to the keyboard. Scanning and code generation and serialization is accomplished on the keyboard through the use of a microprocessor (8035) and a firmware PROM. In the future the microprocessor will become a custom 8048 or 8049 with the firmware masked within the device, eliminating the PROM. The schematic for the keyboard is contained in Section 7 and is KTC number 65-02335.

2.9 VIDEO OPERATION

Sheet 5 of the schematics contains the video generation logic which consists of the PVTC (2672, U86), standard character generator (2732, U97), and the video attribute controller (2673, U96) for alpha display.

The 2673 is programmed by ground and VREF jumpers to divide the dot clock (DCLK) by 9 to form the character clock (CCLK) used by the PVTC.

The PVTC (2672) is programmed during initialize for 100 characters for each raster line (blanking beyond 80 characters), 15 raster lines for each character line (increments the RAM address), and 645 raster lines (blanking beyond 510). This programming results in horizontal syncs (HSYNC) being generated each 51.9 microseconds and vertical syncs being generated each 33.33 milliseconds. With this timing the PVTC steps the video address bus (DADDØ-DADD13) character by character to fetch data from the video memory. In addition the address bus is used to provide the character generators with the line address (slice count) during the blanking interval. DADD4-DADD7 contain the slice count and are strobed into the character generator at the end of the horizontal blanking interval by delayed horizontal sync (DLHSYNC).

During display, VBWR and VWR are false (see Section 2.6 for I/O bus operations) and video RAM enable (VRAME) is true. This enables the video RAM (sheet 5) in the read mode, providing, at its output, the ASCII code and attributes of each character to be displayed.

The character generator receives character codes from display memory, which are latched with the character clock (CCLK), and slice counts from the PVTC which are latched by blank sync. The dot outputs from the character generator is presented to the VAC (video attribute controller, U96.

The video attribute controller serializes the dots presented by the characters generators and modifies the video according to character, line, field, and page attributes. Blank character or field attribute (BLANKA), blink character field attribute (BLINKA), underline character field attribute (ULATT), bold character field attribute (BOLDAT) and reverse character field attribute (RVIDAT) are presented to the 2673 for implementation by the video RAM. Gates U76, sheet 5, allows complete page reverse video (PREV), from the PIO, and cause the cursor to be displayed in video which is reversed from whatever is specified by the character at its present location. The BLANK input, pin 15, allows the VAC to blank video

beyond the active area both vertically and horizontally. BLINKF, pin 17, is the blink rate input which determines the rate at which the VAC will blink video when the blink attribute is specified. DADD10, on pin 16, comes from the PVTC and allows underlining of an entire line rather than character by character as the underline attribute (ULATT) generates. DADD13, on pin 18, indicates that the last raster line of the current character line is finishing. This allows the VAC to extend field attributes beyond the end of the current character line. The video output via TTLVID1 and TTLVID2, allows analog mixing to achieve full intensity, half intensity, white and black backgrounds. Figure 2-3 defines these levels.

TTLVID1	TTLVID2	DEFINITION
0	0	No video on a black background
0	0	Gray video (background) on black background
1	0	Gray video (background) on white background
1	1	Black video on white background or white (foreground) video on black background

Figure 2-3. Video Output Levels

On sheet 4 of the schematics, the two video levels are mixed with gates U103 and Q4 to provide the video output to the monitor. The video output is attenuated by the ladder network R16-R21 to provide a programmable intensity control.

In graphics mode, data is extracted from the graphics RAMS, sheet 9, by the GDC (7220). The GDC is synchronized to the PVTC through the use of the PVTC generated vertical sync, (VSYNC, uPD 7220, U39, pin 4). Graphics RAM data (GMDØ-GMD15) is loaded into the parallel-in, serial-out shift registers, U71 and U81, sheet 7. Serialized graphic data is exclusive or'd with page reverse (GPREV) to form graphics serial register output data (GSRO) which is and'd with alpha numeric data (TTLVID1, TTLVID2) on sheet 5, resulting in composite video (COMVID1, COMVID2) which is sent to the monitor after the brightness control is added. In this manner, both graphics and alpha data can be displayed simultaneously.

Detailed specification sheets on the video chip set are contained in Section 5.

2.10 SELF TEST

The Visual 500/550 executes a self test each time it is powered on. A checksum is calculated and checked against the checksum stored in the last two locations of the Firmware PROMS; a RAM test is executed and the non-volatile RAM is checked. If all are correct the screen is initialized and a cursor is displayed. If either the firmware checksum or RAM test fails, the screen is not initialized and either a black screen or a black screen with a horizontal line in the center results. If the non-volatile RAM fails, the screen is initialized, default set-up parameters are selected, and the bell is sounded twice. In this situation operation is allows, however, it will be necessary to manually set any parameters which differ from default set-up parameters.

If extended diagnostics are enabled, the graphic memory RAMS are checked and a test pattern is displayed on the screen. This test takes a minute and a half to complete. If there is a RAM failure, then the RAM failure is displayed in the following message:

AAAA B P.

The AAAA value is the address of the failure in hex from 0000 through 7FFF. B value is the bit that failed 0 through F and the P is the number of the pass in which the test failed.

Be sure to disable the extended Diagnostics after the test is completed or you have to wait for test to be performed every time the terminal is powered on.

2.11 JUMPER ASSIGNMENTS

Jumpers W1 through W6 are determined by size of the firmware. PROM and jumper configurations are defined in Section 2.4.

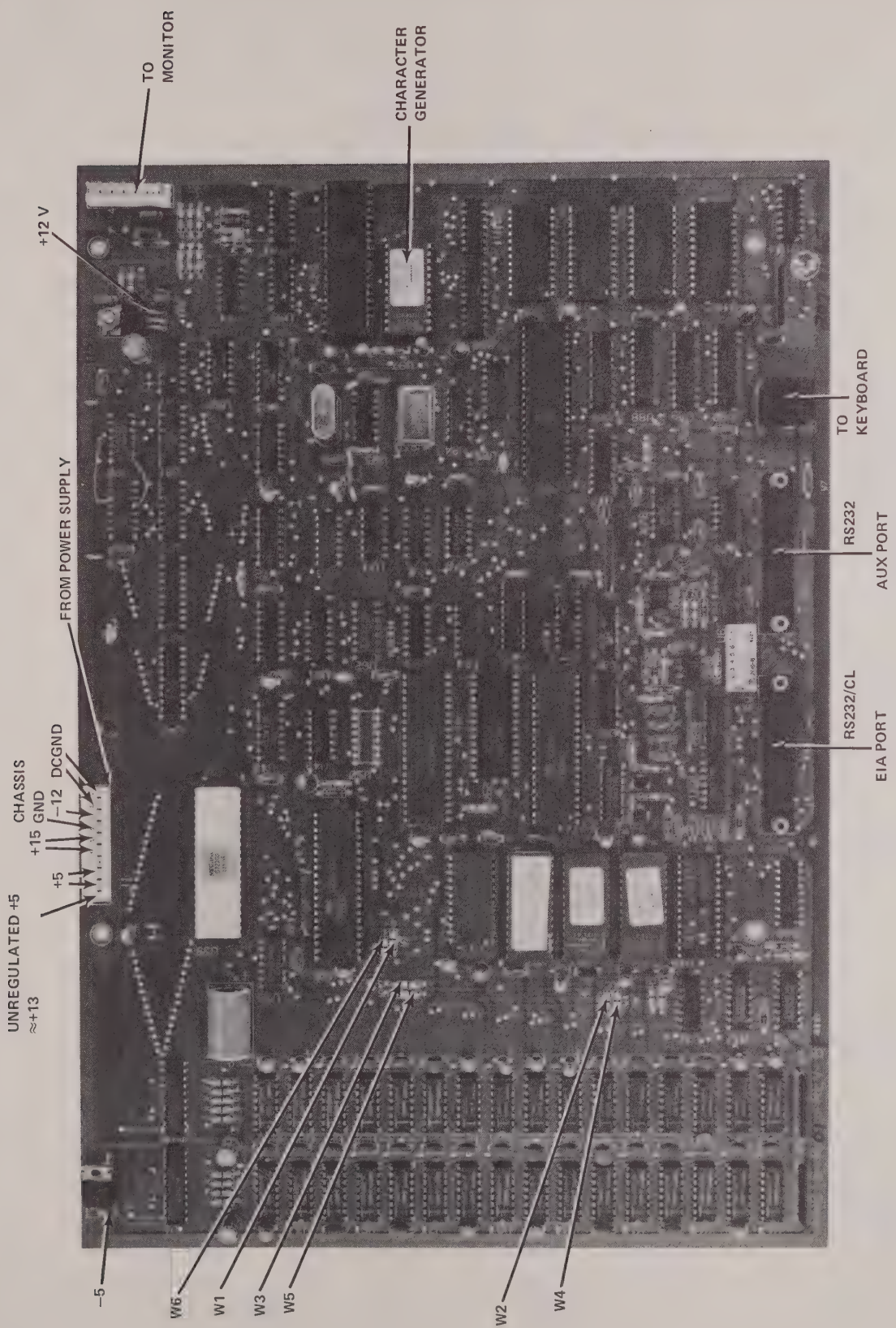


Figure 2-4. Jumper Locations

3. SPARE PARTS AND TOOLS

3.1 SPARE PARTS

Each Visual 500/550 terminal is composed of four major subassemblies which are designed to be serviced on site, by replacing the subassembly.

3.1.1 TV Monitor Subassembly

The Zenith model DS 14NK 153 monitor is provided in the V500/550.

Description	Zenith PN	Visual PN
Monitor Kit (total)	DS14NK153	MN014-020
PCB	A10210	MN013-006
Flyback Transformer	A8814	MN003-001
CRT (P39)	100-727-05	MN014-027
Yoke	A08837	MN001-004

3.1.2 Keyboard Assembly

One keyboard is used on the Visual 500/550. It is manufactured by KTC and is manufactured in the standard US version only. If your keyboard is configured in a foreign national version, it will be necessary to exchange keycaps at the time a spare keyboard is installed. The KTC part number for the keyboard is 65-02335 and Visual's part number is KB 005-015.

3.1.3 Main PCB

The main logic PCB contains all the active components except the power supply components which are located on the power supply subassembly, PA 005-A01.

Description	Visual PN
Power Supply PCB	PA 005-A01
Main PCB	PA 016-B01

PROMS and ROMS which are used on the Main PCB are listed below with their function.

FIRMWARE FOR 550

Function	Location	Visual PN
Firmware	U42	E244-001
Firmware	U43	E244-002
Firmware	U44	E244-003
Firmware	U45	E244-017
Character PROM	U97	E242-085

FIRMWARE FOR 500

Function	Location	Visual PN
Firmware	U42	E244-013
Firmware	U43	E244-014
Firmware	U44	E244-015
Firmware	U45	E244-016
Character PROM	U97	E242-085

All firmware PROMS must be of the same revision.

3.2 SPARE SUBASSEMBLY RECOMMENDATIONS

To service 100 terminals by subassembly exchange, the following subassemblies should be stocked in the quatities shown:

Quantity	Description	Part Number
5	Main PCB	PA016-B01
3	TV Monitor PCB	MN013-006
3	Keyboards	KB005-015
3	Power Supplies	PA005-A01

3.2.1 Active Component Recommendations

The following list contains the active components found on the main PCB and on the Keyboard. Total qualities per terminal and stocking recommendations are indicated. Components used on each of the monitor models are found in Section 7. The recommendations are based on one depot repairing subassemblies from approximately 100 terminals. Components which are either custom or are sufficiently unique so that they are not found on distribution shelves are indicated with an *.

PART	VISUAL P/N	QTY/TERMINAL	RECOMMENDED SPARE/100
74F00	IC050-000	1	10
74F04	IC050-004	3	20
74F32	IC050-032	1	10
74F74	IC050-74	1	10
74F161	IC050-161	1	10
74F174	ICO50-174	1	10
74F175	IC050-175	2	15
74LS00	IC000-000	2	15
74LS04	IC000-004	3	10
74LS08	IC000-008	1	10
74LS32	IC000-032	1	10
74LS51	IC000-051	1	10
74LS74	IC000-074	2	15

PART	VISUAL P/N	QTY/TERMINAL	RECOMMENDED SPARE/100
74LS86	IC000-086	1	10
74LS93	IC000-093	1	10
74LS138	IC000-138	3	20
74L139	IC000-139	2	15
74LS174	IC000-174	1	10
74LS175	IC000-175	2	15
74LS244	IC000-244	3	20
74LS257	IC000-257	1	10
74LS273	IC000-273	1	10
74LS374	IC000-374	4	20
7416	IC010-016	1	10
7417	IC010-017	1	10
7426	IC010-026	1	10
74166	IC010-166	2	10
74S161	IC020-161	1	10
74S175	IC020-175	1	10
2016	IC140-010	5	25
1488	IC340-001	2	15
1489	IC340-002	2	13
*Z80 (uPD780)	IC440-001	1	10
*PIO (uPD8255A-5)	IC440-005	1	10
*Z672	IC440-012	1	10
*Z673	IC440-013	1	10
*MCT-2	IC340-008	2	15
*Dual USART (7201)	IC440-010	1	10
1N914	DA000-001	9	30
7812	VR100-012	1	10
79M05	VR410-005	1	10
*8116T020	IC340-005	2	15
*Battery	BT-000-34	1	10
*uPD 7220 (GDC)	IC440-014	1	10
*OSC. MODULE	IC342-002	1	10
*18.432 MHz	XT020-001	1	10
uPD 444	IC140-005	1	10
PN-3644	TR000-001	2	15
*2673	IC242-085	1	10
8251A	IC440-003	1	10
D416	IC140-009	32	15
*8048	KTC 2208048-161	1	10
74LS14	KTC 2207414-001	1	10
74LS373	KTC 2274373-001	1	10
TIP32	TR020-001	1	10
TIP34	TR030-001	2	15
2N4901	TR010-001	1	10
7805	VR100-005	1	10
7815	VR100-015	1	10
1N5401	DA320-001	4	20
CR1	DA350-001	4	20

3.3 TOOLS

In order to gain access to the Visual 500/550 and to replace any subassembly, only a cross head and a straight blade screwdriver are necessary.

In order to repair any subassembly, only an oscilloscope such as a Tektconix 465 is required. Although not required, a Z80 in circuit emulator may lessen the time required to isolate RAM failures.

4. MNEMONIC LIST

Mnemonic	Sheet	IC	Definition
+5	1	Q2	P.S. sch +5 volts DC
–5	9	VR1	–5 volts DC
+12	9	VR2	+volts DC
–12	1	VR3	P.S. Sch. – 12 volts DC
+15	1	Q4	P.S. Sch. +15 volts DC
AB∅-AB15	several		Address Bus (Z80) Bits ∅-15
ACAS	7	U49	Access dynamic RAM column
ACRAM	1	U51	Activate CMOS RAM (non-volatile memory)
ACTS	1	U51	Allow clear-to-send
ADSTB	8	U92	Address strobe
BLANK A	6	U101	Video blank video attribute
BLANK	5	U86	Video blanking
BLINK A	6	U101	Video blank video attribute
BOLDAT	6	U101	Bold video attribute
BRD∅-BRD4	1	U51	Video flop (blink rate)
BT1	2		Batter 3.4
BUSACK	6	U40	Bus acknowledge (not used)
BUSRQ	6	U40	Bus request (not used)
CAS	8	U48	Dynamic RAM column address strobe
CASE 1	7	U36	Dynamic RAM lower bank select
CASE 2	7	U36	Dynamic RAM upper bank select
CCLK	5	U96	Character clock (1.925 MHz)
CINT	4	U52	Combined interrupt
CLOOP	3	U68	Current loop data (receive)
COM VID 1	5	U70	Combined video level 1
COM VID 2	5	U70	Combined video level 2
CTS	4	U53	Clear to send
CURSOR	5	U86	Cursor
DADD0-DADD13	5	U86	Display address (video)
DATACLK	5	U83	Data rate clock (4.33 MHz)
DB∅-DB7	several		Z8∅
DBIN	7	U39	Data buss input
DCD	3	U58	Detected carrier detect
DSR	3	U58	Data set ready
DTR	4	U53	Data terminal ready
DWR	1	U73	Delay write
EGVID	1	U51	Enable graphic video
GBLANK	7	U39	Graphic blank

Mnemonic	Sheet	IC	Definition
GRAFAT	6	U101	Graphic attribute
GMAØ-GMA6	7	U18	Graphic memory address
GMDØ-GMD15	9	U47 & U459	Graphic data memory
GMWR	8	U82	Graphic memory write
GPREV	8	U60	Graphic page reverse video
GSRO	7	U80	Graphic serial out
GSRLD	8	U91	Graphic serial load
GTXD	3	U57	Gated transmitt data
HALT	1	U40	Halt state
HSYNC	5	U86	Horizontal sync
HSYNCD	8	U91	Horizontal sync delay
IOREQ	1	U40	I/O request
KBCLK	4	U66	Keyboard clock
KBRD	4	U52	Keyboard receive data
KBXD	4	U52	Keyboard transmitt data
LDE	1	U51	Local data enable
MREQ	1	U40	Memory request
MUX	8	U48	Multiplex address select
NMI	see VIDIPT		Non maskable interrupt
ODEVFL	1	U51	Odd/even field (frame)
ORAS	7	U39	Output row address strobe
PBUSY	4	U52	Printer busy
PDTR	4	U52	Printer data terminal ready
PIPT	4	U57	Printer interrupt
PPRES	3	U78	Printer presort
PCLOCK	5	U74	Processor clock (2.165 MHz)
PREV	1	U51	Page reverse video
PRXD	4	U53	Printer receive data
PTXD	4	U53	Printer transmitt data
RAMSEL	1	U37	RAM select
RAS	8	U49	Dynamic RAM address strobe
RD	1	U40	Z80 read
RESET	6	U49	Reset
RFSH	1	U40	Refresh for dynamic RAMs
ROMØ-ROM2	1	U37	ROM select
ROM3	1	U38	ROM select
RTS	4	U53	Request-to-send
RXCLK	4	U66	Receive clock (asynchronous)
RVIDATI	6	U101	Reverse video attribute
RXCLK	4	U66	Receive clock
RXD	3	U64	Receive data
RXT	3	U69	Receive clock (sychronous)
RDE	1	U51	Read data enable
SBRGØ	1	U62	Select baud rate generator 0
SBRG1	1	U62	Select baud rate generator 1
SCCD	3	U69	Secondary channel carrier detect

Mnemonic	Sheet	IC	Definition
SCRTS	4	U62	Secondary channel request to send
SMPSC	1	U62	Select multi-protocal serial controller
SPIO	1	U62	Select parallel I/O
SPUSART	1	U62	Select printer USART
SVARD	1	U77	Select video attribute read
SVAWR	1	U77	Select video attribute write
SVDRD	1	U77	Select video data read
SVDWR	1	U77	Select video data write
SVTAC	1	U62	Select video timing and control chip
SYNC	1	U51	Synchronous select
SGDCR	1	U61	Select graphic display control read
SGDCW	1	U61	Select graphic display control write
TTLVID1	5	U95	TTL video level 1
TTLVID2	5	U95	TTL video level 2
TXCLK	4	U65	Transmit clock (asynchronous)
TXD	4	U53	Transmit data
TXE	1	U51	Transmit enable
TXT	3	U69	Transmit clock (synchronous)
ULATT	6	U101	Underline attribute
VBWR	5	U86	Video buffer write
VDBØ-VDB7	6	U87	Video data buss Ø-7
VIDEO	4	Q4	Video output to monitor
VDIPT	5	U86	Video interrupt
VRAME	5	U86	Video RAM enable
VREFA	5	U75	Voltage reference A5
VRD	6	U104	Video read
VSYNC	5	U86	Vertical sync
VWR	5	U86	Video write
WR	1	U40	Write

5. I.C. DATA SHEETS

Included in this section are specifications for the following I.C.'s.

Z80 (UPD 780)	Z80 CPU
UPD 8251A	USART
UPD 8255A-5	PIO
7201	Dual USART
2672	PVTC
2673	VAC
2670/2672/2673	Application Note
UPD 416	16Kx1 Dynamic RAM
UPD 444	1Kx4 CMOS RAM
TMM 2018/UPD 4016	2Kx8 Static RAM
8116T-028	Baud Rate Generator
IC244-085	Character Generator PROM
PD7220/GDC	Graphic Display Controller

8-BIT N-CHANNEL MICROPROCESSOR COMPLETELY Z80™ COMPATIBLE

DESCRIPTION

The μPD780 and μPD780-1 processors are single chip microprocessors developed from third generation technology. Their increased computational power produces higher system through-put and more efficient memory utilization, surpassing that of any second generation microprocessor. The single voltage requirement of the μPD780 and μPD780-1 processors makes it easy to implement them into a system. All output signals are fully decoded and timed to either standard memory or peripheral circuits. An N-channel, ion implanted, silicon gate MOS process is utilized in implementing the circuit.

The block diagram shows the functions of the processor and details the internal register structure. The structure contains 26 bytes of Read/Write (R/W) memory available to the programmer. Included in the registers are two sets of six general purpose registers, which may be used as 8-bit registers individually, or as 16-bit register pairs. Also included are two sets of accumulator and flag registers.

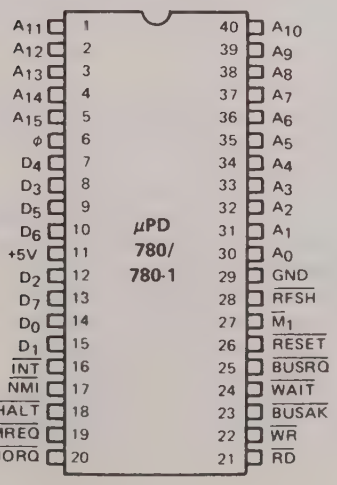
Through a group of exchange instructions the programmer has access to either set of main or alternate registers. The alternate register permits foreground/background mode of operation, or may be used for fast interrupt response. A 16-bit stack pointer is also included in each processor, simplifying implementation of multiple level interrupts, permitting unlimited subroutine nesting, and simplifying many types of data handling.

The two 16-bit index registers simplify implementation of relocatable code and manipulation of tabular data. The Refresh register will automatically refresh external dynamic memories. A powerful interrupt response mode will use the I register to form the upper 8-bits of a pointer to an interrupt service address table, while the interrupting apparatus supplies the lower 8-bits of the pointer. An indirect call will then be made to service this address.

FEATURES

- Single Chip, N-Channel Silicon Gate Processor
- 158 Instructions — Including all 78 of the 8080A Instructions, Permitting Total Software Compatibility
- New 4-, 8-, and 16-Bit Operations Featuring Useful Addressing Modes such as Indexed, Bit and Relative
- 17 Internal Registers
- Three Modes of Rapid Interrupt Response, and One Non-Maskable Interrupt
- Directly Connects Standard Speed Dynamic or Static Memories, with Minimum Support Circuitry
- Single-Phase +5 Volt Clock and 5 VDC Supply
- TTL Compatibility
- Automatic Dynamic RAM Refresh Circuitry
- Available in Plastic Package

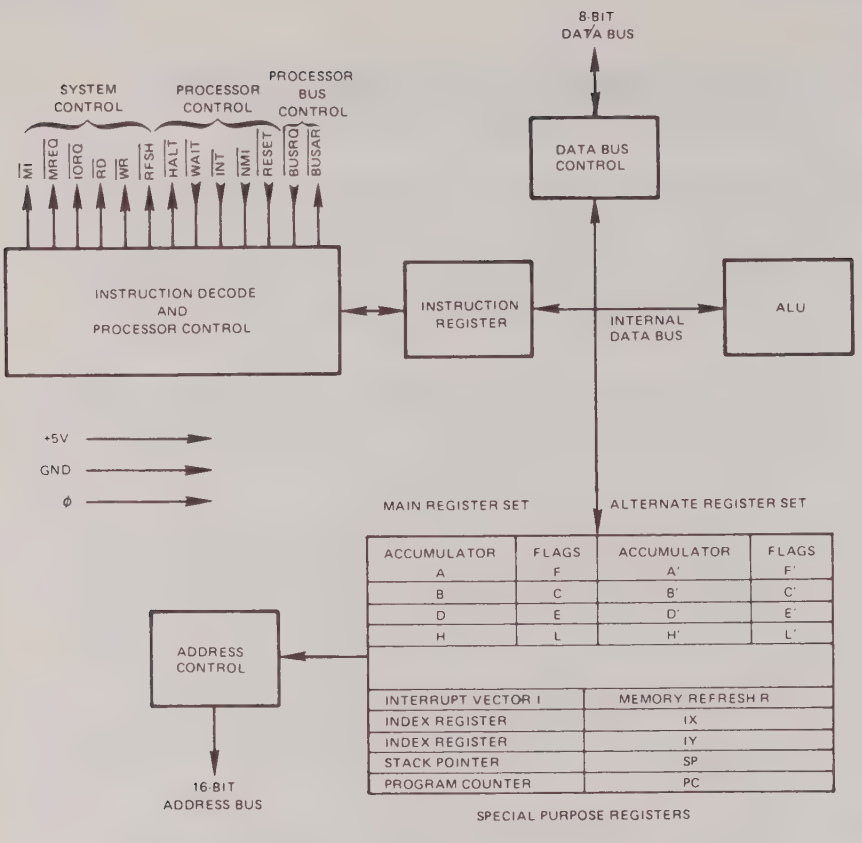
PIN CONFIGURATION



TM: Z80 is a registered trademark of Zilog, Inc.

173 Worcester Street/Wellesley, Massachusetts 02181 Telephone 617/237-1910 TWX: 710-383-1745

BLOCK DIAGRAM



PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
1-5, 30-40	A_0-A_{15}	Address Bus	3-State Output, active high. Pins A_0-A_{15} constitute a 16-bit address bus, which provides the address for memory and I/O device data exchanges. Memory capacity 65,536 bytes. A_0-A_7 is also needed as refresh cycle.
7-10, 12-15	D_0-D_7	Data Bus	3-State input/output, active high. Pins D_0-D_7 compose an 8-bit, bidirectional data bus, used for data exchanges with memory and I/O devices.
27	$\overline{M_1}$	Machine Cycle One	Output, active low. $\overline{M_1}$ indicates that the machine cycle in operation is the op code fetch cycle of an instruction execution.
19	$\overline{MREQ}$	Memory Request	3-State output, active low. $\overline{MREQ}$ indicates that a valid address for a memory read or write operation is held in the address.
20	$\overline{IORQ}$	Input/Output Request	3-State output, active low. The I/O request signal indicates that the lower half of the address bus holds a valid address for an I/O read or write operation. The $\overline{IORQ}$ signal is also used to acknowledge an interrupt command, indicating that an interrupt response vector can be placed on the data bus.
21	$\overline{RD}$	Memory Read	3-State output, active low. $\overline{RD}$ indicates that the processor is requesting data from memory or an I/O device. The memory or I/O device being addressed should use this signal to gate data onto the data bus.

PIN IDENTIFICATION (CONT.)

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
22	$\overline{WR}$	Memory Write	3-State output, active low. The memory write signal indicates that the processor data bus is holding valid data to be stored in the addressed, memory or I/O device.
28	$\overline{RFSH}$	Refresh	Output, active low. $\overline{RFSH}$ indicates that a refresh address for dynamic memories is being held in the lower 7-bits of the address bus. The $\overline{MREQ}$ signal should be used to implement a refresh read to all dynamic memories.
18	$\overline{HALT}$	Halt State	Output, active low. $\overline{HALT}$ indicates that the processor has executed a HALT software instruction, and will not resume operation until either a non-maskable or a maskable (with mask enabled) interrupt has been implemented. The processor will execute NOP's while halted, to maintain memory refresh activity.
24	$\overline{WAIT}$	Wait	Input, active low. $\overline{WAIT}$ indicates to the processor that the memory or I/O devices being addressed are not ready for a data transfer. As long as this signal is active, the processor will reenter wait states.
16	$\overline{INT}$	Interrupt Request	Input, active low. The $\overline{INT}$ signal is produced by I/O devices. The request will be honored upon completion of the current instruction, if the interrupt enable flip-flop (IFF) is enabled by the internal software. There are three modes of interrupt response. Mode 0 is identical to 8080 interrupt response mode. The Mode 1 response is a restart location at 0038_H. Mode 2 is for simple vectoring to an interrupt service routine anywhere in memory.
17	$\overline{NMI}$	Non-Maskable Interrupt	Input, active low. The non-maskable interrupt has a higher priority than $\overline{INT}$. It is always acknowledged at the end of the current instruction, regardless of the status of the interrupt enable flip-flop. When the $\overline{NMI}$ signal is given, the μPD780 processor automatically restarts to location 0066_H.
26	$\overline{RESET}$	Reset	Input, active low. The $\overline{RESET}$ signal causes the processor to reset the interrupt enable flip-flop (IFF), clear PC and I and R registers, and set interrupt to 8080A mode. During the reset time, the address bus and data bus go to a state of high impedance, and all control output signals become inactive, after which processing continues at 0000H.
25	$\overline{BUSRQ}$	Bus Request	Input, active low. $\overline{BUSRQ}$ has a higher priority than $\overline{NMI}$, and is always honored at the end of the current machine cycle. It is used to allow other devices to take control over the processor address bus, data bus signals; by requesting that they go to a state of high impedance.
23	$\overline{BUSAK}$	Bus Acknowledge	Output, active low. $\overline{BUSAK}$ is used to inform the requesting device that the processor address bus, data bus and 3-state control bus signals have entered a state of high impedance, and the external device can now take control of these signals.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Voltage on any Pin	−0.3 to +7 Volts ①
Power Dissipation	1.5W

Note: ① With Respect to Ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 5% unless otherwise specified.

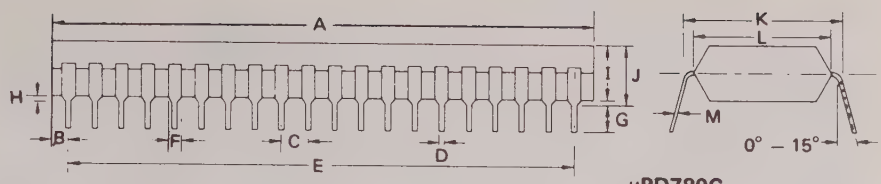
PARAMETER		SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Input Low Voltage		V_{ILC}	-0.3		0.45	V	
Clock Input High Voltage		V_{IHC}	V_{CC}-0.2		V_{CC}	V	
Input Low Voltage		V_{IL}	-0.3		0.8	V	
Input High Voltage		V_{IH}	2.0		V_{CC}	V	
Output Low Voltage		V_{OL}			0.4	V	I_{OL} = 1.8 mA
Output High Voltage		V_{OH}	2.4			V	I_{OH} = -250 μA
Power Supply Current	μPD780	I_{CC}			150	mA	t_c = 400 ns
	μPD780-1	I_{CC}		90	200	mA	t_c = 250 ns
Input Leakage Current		I_{LI}			10	μA	V_{IN} = 0 to V_{CC}
Tri-State Output Leakage Current in Float		I_{LOH}			10	μA	V_{OUT} = 2.4 to V_{CC}
Tri-State Output Leakage Current in Float		I_{LOL}			-10	μA	V_{OUT} = 0.4 V
Data Bus Leakage Current in Input Mode		I_{LD}			±10	μA	$0 \leq V_{IN} \leq V_{CC}$

CAPACITANCE

T_a = 25°C

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Capacitance	C_ϕ			35	pF	f_c = 1 MHz
Input Capacitance	C_{IN}			5	pF	Unmeasured Pins
Output Capacitance	C_{OUT}			10	pF	Returned to Ground

PACKAGE OUTLINES
μPD780C/D



μPD780C
μPD780C-1
(Plastic)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

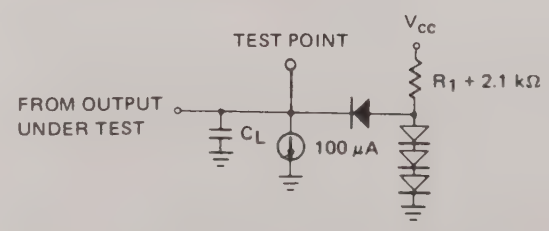
AC CHARACTERISTICS

T_a = 0°C to +70°C, V_{CC} = +5V ± 5%, unless otherwise specified

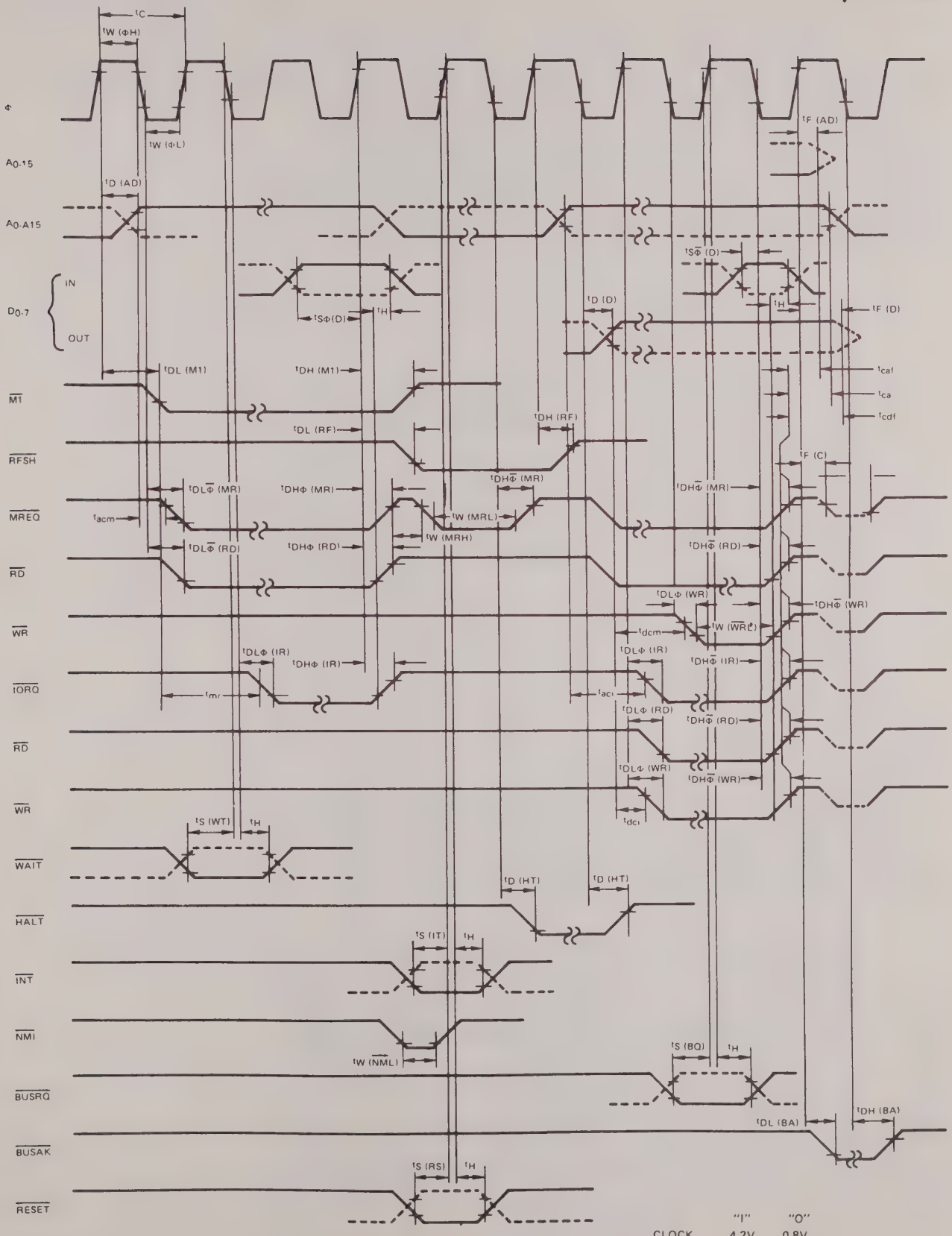
PARAMETER	SYMBOL	LIMITS μPD780 MIN	LIMITS μPD780 MAX	LIMITS μPD780-1 MIN	LIMITS μPD780-1 MAX	UNIT	TEST CONDITIONS
Clock Period	t_c	0.4	⑫	0.25	⑫	μs	
Clock Pulse Width, Clock High	$t_w(\Phi H)$	180		110		ns	
Clock Pulse Width, Clock Low	$t_w(\Phi L)$	180	2000	110	2000	ns	
Clock Rise and Fall Time	t_r, t_f		30		30	ns	
Address Output Delay	$t_{D(AD)}$		145		110	ns	
Delay to Float	$t_{F(AD)}$		110		90	ns	
Address Stable Prior to $\overline{MREQ}$ (Memory Cycle)	t_{acm}	①		①		ns	C_L = 50 pF
Address Stable Prior to $\overline{IORQ}$, $\overline{RD}$ or $\overline{WR}$ (I/O Cycle)	t_{aci}	②		②		ns	
Address Stable from $\overline{RD}$ or $\overline{WR}$	t_{ca}	③		③		ns	
Address Stable from $\overline{RD}$ or $\overline{WR}$ During Float	t_{caf}	④		④		ns	
Data Output Delay	$t_{D(D)}$		230		150	ns	
Delay to Float During Write Cycle	$t_{F(D)}$		90		90	ns	
Data Setup Time to Rising Edge of Clock During M1 Cycle	$t_{S\Phi(D)}$	50		35		ns	
Data Setup Time to Falling Edge of Clock During M2 to M5 Cycles	$t_{S\bar{\Phi}(D)}$	60		50		ns	C_L = 200 pF
Data Stable Prior to $\overline{WR}$ (Memory Cycle)	t_{dcm}	⑤		⑤		ns	
Data Stable Prior to $\overline{WR}$ (I/O Cycle)	t_{dci}	⑥		⑥		ns	
Data Stable from $\overline{WR}$	t_{cdf}	⑦		⑦		ns	
Any Hold Time for Setup Time	t_H	0			0	ns	
$\overline{MREQ}$ Delay from Falling Edge of Clock to $\overline{MREQ}$ Low	$t_{DL\bar{\Phi}(MR)}$		100		85	ns	
$\overline{MREQ}$ Delay from Rising Edge of Clock to $\overline{MREQ}$ High	$t_{DH\Phi(MR)}$		100		85	ns	
$\overline{MREQ}$ Delay from Falling Edge of Clock to $\overline{MREQ}$ High	$t_{DH\bar{\Phi}(MR)}$		100		85	ns	
Pulse Width, $\overline{MREQ}$ Low	$t_{w(\overline{MRL})}$	⑧		⑧		ns	
Pulse Width, $\overline{MREQ}$ High	$t_{w(\overline{MRH})}$	⑨		⑨		ns	
$\overline{IORQ}$ Delay from Rising Edge of Clock to $\overline{IORQ}$ Low	$t_{DL\Phi(IR)}$		90		75	ns	
$\overline{IORQ}$ Delay from Falling Edge of Clock to $\overline{IORQ}$ Low	$t_{DL\bar{\Phi}(IR)}$		110		85	ns	
$\overline{IORQ}$ Delay from Rising Edge of Clock to $\overline{IORQ}$ High	$t_{DH\Phi(IR)}$		100		85	ns	
$\overline{IORQ}$ Delay from Falling Edge of Clock to $\overline{IORQ}$ High	$t_{DH\bar{\Phi}(IR)}$		110		85	ns	C_L = 50 pF
$\overline{RD}$ Delay from Rising Edge of Clock to $\overline{RD}$ Low	$t_{DL\Phi(RD)}$		100		85	ns	
$\overline{RD}$ Delay from Falling Edge of Clock to $\overline{RD}$ Low	$t_{DL\bar{\Phi}(RD)}$		130		95	ns	
$\overline{RD}$ Delay from Rising Edge of Clock to $\overline{RD}$ High	$t_{DH\Phi(RD)}$		100		85	ns	
$\overline{RD}$ Delay from Falling Edge of Clock to $\overline{RD}$ High	$t_{DH\bar{\Phi}(RD)}$		110		85	ns	
$\overline{WR}$ Delay from Rising Edge of Clock to $\overline{WR}$ Low	$t_{DL\Phi(WR)}$		80		65	ns	
$\overline{WR}$ Delay from Falling Edge of Clock to $\overline{WR}$ Low	$t_{DL\bar{\Phi}(WR)}$		90		80	ns	
$\overline{WR}$ Delay from Falling Edge of Clock to $\overline{WR}$ High	$t_{DH\Phi(WR)}$		100		80	ns	
Pulse Width to $\overline{WR}$ Low	$t_{w(\overline{WRL})}$	⑩		⑩		ns	
$\overline{M1}$ Delay from Rising Edge of Clock to $\overline{M1}$ Low	$t_{DL(M1)}$		130		100	ns	C_L = 30 pF
$\overline{M1}$ Delay from Rising Edge of Clock to $\overline{M1}$ High	$t_{DH(M1)}$		130		100	ns	
$\overline{RFSH}$ Delay from Rising Edge of Clock to $\overline{RFSH}$ Low	$t_{DL(RF)}$		180		130	ns	
$\overline{RFSH}$ Delay from Rising Edge of Clock to $\overline{RFSH}$ High	$t_{DH(RF)}$		150		120	ns	
$\overline{WAIT}$ Setup Time to Falling Edge of Clock	$t_{s(WT)}$	70		70		ns	
$\overline{HALT}$ Delay Time from Falling Edge of Clock	$t_{D(HT)}$		300		300	ns	C_L = 50 pF
$\overline{INT}$ Setup Time to Rising Edge of Clock	$t_{s(IT)}$	80		80		ns	
Pulse Width, $\overline{NMI}$ Low	$t_{w(\overline{NML})}$	80		80		ns	
$\overline{BUSRQ}$ Setup Time to Rising Edge of Clock	$t_{s(BQ)}$	80		50		ns	
$\overline{BUSAK}$ Delay from Rising Edge of Clock to $\overline{BUSAK}$ Low	$t_{DL(BA)}$		120		100	ns	C_L = 50 pF
$\overline{BUSAK}$ Delay from Falling Edge of Clock to $\overline{BUSAK}$ High	$t_{DH(BA)}$		110		100	ns	
$\overline{RESET}$ Setup Time to Rising Edge of Clock	$t_{s(RS)}$	90		60		ns	
Delay to Float ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ and $\overline{WR}$)	$t_{F(C)}$		100		80	ns	
$\overline{M1}$ Stable Prior to $\overline{IORQ}$ (Interrupt Ack.)	t_{mr}	⑪		⑪		ns	

Notes
① $t_{acm} = t_w(\Phi H) + t_f - 65$ (75)*
② $t_{aci} = t_c - 70$ (80)*
③ $t_{ca} = t_w(\Phi L) + t_r - 50$ (40)*
④ $t_{caf} = t_w(\Phi L) + t_r - 45$ (60)*
⑤ $t_{dcm} = t_c - 170$ (210)*
⑥ $t_{dci} = t_w(\Phi L) + t_r - 170$ (210)*
⑦ $t_{cdf} = t_w(\Phi L) + t_r - 70$ (80)*
⑧ $t_{w(\overline{MRL})} = t_c - 30$ (40)*
⑨ $t_{w(\overline{MRH})} = t_w(\Phi H) + t_f - 20$ (30)*
⑩ $t_{w(\overline{WR})} = t_c - 30$ (40)*
⑪ $t_{mr} = 2t_c + t_w(\Phi H) + t_f - 65$ (80)*
⑫ $t_c = t_w(\Phi H) + t_w(\Phi L) + t_r + t_f$

*These values apply to the μPD780



LOAD CIRCUIT FOR OUTPUT

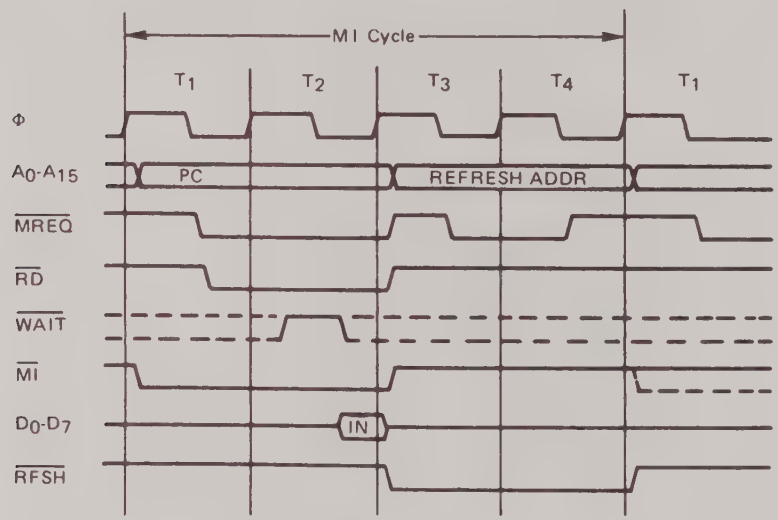


	"I"	"O"
CLOCK	4.2V	0.8V
OUTPUT	2.0V	0.8V
INPUT	2.0V	0.8V
FLOAT	ΔV	±0.5V

Note: ① Timing measurements are made at the following voltages unless otherwise specified:

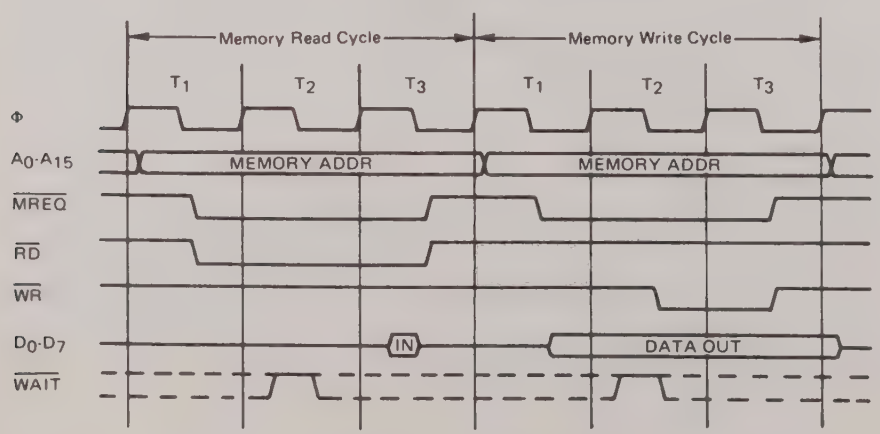
Instruction Op Code Fetch

The contents of the program counter (PC) are placed on the address bus at the start of the cycle. $\overline{MREQ}$ goes active one-half clock cycle later, and the falling edge of this signal can be used directly as a chip enable to dynamic memories. The memory data should be enabled onto the processor data bus when $\overline{RD}$ goes active. The processor takes data with the rising edge of the clock state T_3. The processor internally decodes and executes the instruction, while clock states T_3 and T_4 of the fetch cycle are used to refresh dynamic memories. The refresh control signal $\overline{RFSH}$ indicates that a refresh read should be done to all dynamic memories.



Memory Read or Write Cycles

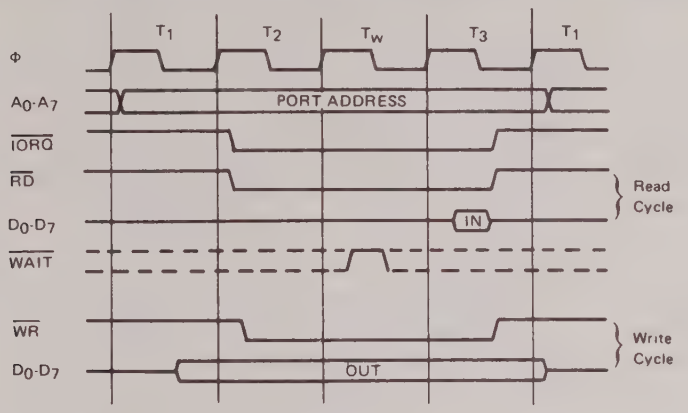
This diagram illustrates the timing of memory read or write cycles other than an op code fetch (M_1 cycle). The function of the $\overline{MREQ}$ and $\overline{RD}$ signals is exactly the same as in the op code fetch cycle. When a memory write cycle is implemented, the $\overline{MREQ}$ becomes active and is used directly as a chip enable for dynamic memories, when the address bus is stable. The $\overline{WR}$ line is used directly as a R/W pulse to any type of semiconductor memory, and is active when data on the data bus is stable.



TIMING WAVEFORMS (CONT.)

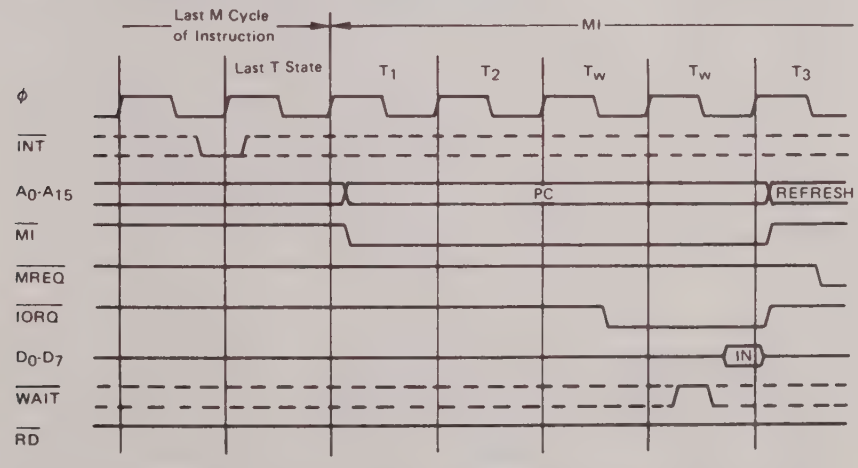
Input or Output Cycles

This illustrates the timing for an I/O read or I/O write operation. A single wait-state (T_W) is automatically inserted in I/O operations to allow sufficient time for an I/O port to decode its address and activate the $\overline{WAIT}$ line, if necessary.



Interrupt Request/Acknowledge Cycle

The processor samples the interrupt signal with the rising edge of the last clock at the end of any instruction. A special M_1 cycle is started when an interrupt is accepted. During the M_1 cycle, the $\overline{IORQ}$ (instead of $\overline{MREQ}$) signal becomes active, indicating that the interrupting device can put an 8-bit vector on the data bus. Two wait states (T_W) are automatically added to this cycle. This makes it easy to implement a ripple priority interrupt scheme.



INSTRUCTION SET

The following summary shows the assembly language mnemonic and the symbolic operation performed by the instructions of the μPD780 and μPD780-1 processors. The instructions are divided into 16 categories:

Miscellaneous Group	8-Bit Loads
Rotates and Shifts	16-Bit Loads
Bit Set, Reset and Test	Exchanges
Input and Output	Memory Block Moves
Jumps	Memory Block Searches
Calls	8-Bit Arithmetic and Logic
Restarts	16-Bit Arithmetic
Returns	General Purpose Accumulator and Flag Operations

The addressing Modes include combinations of the following:

Indexed	Immediate
Register	Immediate Extended
Implied	Modified Page Zero
Register Indirect	Relative
Bit	Extended

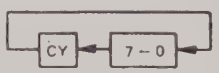
INSTRUCTION SET TABLE

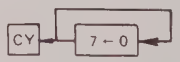
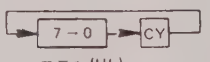
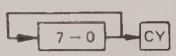
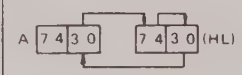
MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
ADC HL, ss	HL ← HL + ss + CY	Add with carry reg. pair ss to HL	1	11	↕	↕	V	↕	0	X	11 101 101 Ⓐ 01 ss1 010
ADC A, r	A ← A + r + CY	Add with carry Reg. r to ACC	1	4	↕	↕	V	↕	0	↕	10 001 rrr Ⓑ
ADC A,n	A ← A + n + CY	Add with carry value n to ACC		7	↕	↕	V	↕	0	↕	11 001 110 nn nnn nnn
ADC A, (HL)	A ← A + (HL) + CY	Add with carry loc. (HL) to ACC		7	↕	↕	V	↕	0	↕	10 001 110
ADC A, (IX + d)	A ← A + (IX + d) + CY	Add with carry loc. (IX + d) to ACC		19	↕	↕	V	↕	0	↕	11 011 101 10 001 110 dd ddd ddd
ADC A, (IY + d)	A ← A + (IY + d) + CY	Add with carry loc. (IY + d) to ACC		19	↕	↕	V	↕	0	↕	11 111 101 10 001 110 dd ddd ddd
ADD A, n	A ← A + n	Add value n to ACC	2	7	↕	↕	V	↕	0	↕	11 000 110 nn nnn nnn
ADD A, r	A ← A + r	Add Reg. r to ACC	1	4	↕	↕	V	↕	0	↕	10 000 rrr Ⓑ
ADD A, (HL)	A ← A + (HL)	Add location (HL) to ACC	1	7	↕	↕	V	↕	0	↕	10 000 110
ADD A, (IX + d)	A ← A + (IX + d)	Add location (IX + d) to ACC	3	19	↕	↕	V	↕	0	↕	11 011 101 10 000 110 dd ddd ddd
ADD A, (IY + d)	A ← A + (IY + d)	Add location (IY + d) to ACC	3	19	↕	↕	V	↕	0	↕	11 111 101 10 000 110 dd ddd ddd
ADD HL, ss	HL ← HL + ss	Add Reg. pair ss to HL	1	11	↕	•	•	•	0	X	00 ss 1 001 Ⓐ
ADD IX, pp	IX ← IX + pp	Add Reg. pair pp to IX	2	15	↕	•	•	•	0	X	11 011 101 Ⓒ 00 pp1 001
ADD IY, rr	IY ← IY + rr	Add Reg. pair rr to IY	2	15	↕	•	•	•	0	X	11 111 101 Ⓓ 00 rr1 001
AND r	A ← A∧r	Logical 'AND' of Reg. r ∧ ACC		4	0	↕	P	↕	0	↕	10 100 rrr Ⓑ
AND n	A ← A∧n	Logical 'AND' of value n ∧ ACC		7	0	↕	P	↕	0	↕	11 100 110 nn nnn nnn
AND (HL)	A ← A∧(HL)	Logical 'AND' of loc. (HL) ∧ ACC		7	0	↕	P	↕	0	↕	10 100 110
AND (IX + d)	A ←A∧(IX + d)	Logical 'AND' of loc. (IX + d) ∧ ACC		19	0	↕	P	↕	0	↕	11 011 101 10 100 110 dd ddd ddd
AND (IY + d)	A ←A∧(IY + d)	Logical 'AND' of loc. (IY + d) ∧ ACC		19	0	↕	P	↕	0	↕	11 111 101 10 100 110 dd ddd ddd
BIT b, (HL)	Z ← $(\overline{HL})_b$	Test BIT b of location (HL)	2	12	•	↕	X	X	0	1	11 001 011 Ⓔ 01 bbb 110
BIT b, (IX + d)	Z ← $(\overline{IX + d})_b$	Test BIT b at location (IX + d)	4	20	•	↕	X	X	0	1	11 011 101 Ⓔ 11 001 011 dd ddd ddd 01 bbb 110
BIT b, (IY + d)	Z ← $(\overline{IY + d})_b$	Test BIT b at location (IY + d)	4	20	•	↕	X	X	0	1	11 111 101 Ⓔ 11 001 011 dd ddd ddd 01 bbb 110
BIT b, r	Z ← $\overline{r}_b$	Test BIT of Reg. r	2	8	•	↕	X	X	0	1	11 001 011 01 bbb rrr Ⓑ Ⓔ
CALL cc, nn	If condition cc false continue, else same as CALL nn	Call subroutine at location nn if condition cc is true	3	10	•	•	∘	•	•	•	11 ←cc→ 100 Ⓗ nn nnn nnn nn nnn nnn
CALL nn	(SP − 1) ← PC_H (SP − 2) ← PC_L PC ← nn	Unconditional call subroutine at location nn	3	17	•	•	•	•	•	•	11 001 101 nn nnn nnn nn nnn nnn
CCF	CY ← CY	Complement carry flag	1	4	↕	•	•	•	0	X	00 111 111
CP r	A − r	Compare Reg. r with ACC		4	↕	↕	V	↕	1	↕	10 111 rrr Ⓑ
CP n	A − n	Compare value n with ACC		7	↕	↕	V	↕	1	↕	11 111 110 nn nnn nnn
CP (HL)	A − (HL)	Compare loc. (HL) with ACC		7	↕	↕	V	↕	1	↕	10 111 110
CP (IX + d)	A − (IX + d)	Compare loc. (IX + d) with ACC		19	↕	↕	V	↕	1	↕	11 011 101 10 111 110 dd ddd ddd
CP (IY + d)		Compare loc. (IY + d) with ACC		19	↕	↕	V	↕	1	↕	11 111 101 10 111 110 dd ddd ddd
CPD	A − (HL) HL ← HL − 1 BC ← BC − 1	Compare location (HL) and ACC, decrement HL and BC	2	16	•	↕②	↕①	↕	1	↕	11 101 101 10 101 001
CPDR	A − (HL) HL ← HL − 1 BC ← BC − 1 until A = (HL) or BC = 0	Compare location (HL) and ACC, decrement HL and BC, repeat until BC = 0	2	21 if BC = 0 and A ≠ (HL) 16 if BC = 0 or A = (HL)	•	↕②	↕①	↕	1	↕	11 101 101 10 111 001

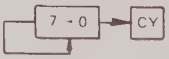
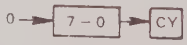
MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
CPI	A – (HL) HL ← HL + 1 BC ← BC – 1	Compare location (HL) and ACC, increment HL and decrement BC	2	16	•	↕②	↕①	↕	1	↕	11 101 101 10 100 001
CPIR	A – (HL) HL ← HL + 1 BC ← BC – 1 until A = (HL) or BC = 0	Compare location (HL) and ACC, increment HL, decrement BC Repeat until BC = C	2	21 if BC = 0 and A ≠ (HL) 16 if BC = 0 or A = (HL)	•	↕②	↕①	↕	1	↕	11 101 101 10 110 001
CPL	A ← A	Complement ACC (1's comp.)	1	4	•	•	•	•	1	1	00 101 111
DAA		Decimal adjust ACC	1	4	↕	↕	P	↕	•	↕	00 100 111
DEC r	r ← r – 1	Decrement Reg. r		4	•	↕	V	↕	1	↕	00 rrr 101Ⓑ
DEC (HL)	(HL) ← (HL) – 1	Decrement loc. (HL)		11	•	↕	V	↕	1	↕	00 110 101
DEC (IX + d)	(IX + d) ← (IX + d) – 1	Decrement loc. (IX + d)		23	•	↕	V	↕	1	↕	11 011 101 00 110 101 dd ddd ddd
DEC (IY + d)	(IY + d) ← (IY + d) – 1	Decrement loc. (IY + d)		23	•	↕	V	↕	1	↕	11 111 101 00 110 101 dd ddd ddd
DEC IX	IX ← IX – 1	Decrement IX	2	10	•	•	•	•	•	•	11 011 101 00 101 011
DEC IY	IY ← IY – 1	Decrement IY	2	10	•	•	•	•	•	•	11 111 101 00 101 011
DEC ss	ss ← ss – 1	Decrement Reg. pair ss	1	6	•	•	•	•	•	•	00 ss1 011Ⓐ
DI	IFF ← 0	Disable interrupts	1	4	•	•	•	•	•	•	11 110 011
DJNZ, e	B ← B – 1 if B = 0 continue if B ≠ 0 PC ← PC + e	Decrement B and jump relative if B = 0	2	8	•	•	•	•	•	•	00 010 000 ◄—e-2—►
EI	IFF ← 1	Enable interrupts	1	4	•	•	•	•	•	•	11 111 011
EX (SP), HL	H ↔ (SP + 1) L ↔ (SP)	Exchange the location (SP) and HL	1	19	•	•	•	•	•	•	11 100 011
EX (SP), IX	IX_H ↔ (SP + 1) IX_L ↔ (SP)	Exchange the location (SP) and IX	2	23	•	•	•	•	•	•	11 011 101 11 100 011
EX (SP), IY	IY_H ↔ (SP + 1) IY_L ↔ (SP)	Exchange the location (SP) and IY	2	23	•	•	•	•	•	•	11 111 101 11 100 011
EX AF, AF'	AF ↔ AF'	Exchange the contents of AF AF	1	4	•	•	•	•	•	•	00 001 000
EX DE, HL	DE ↔ HL	Exchange the contents of DE and HL	1	4	•	•	•	•	•	•	11 101 011
EXX	BC ↔ BC' DE ↔ DE' HL ↔ HL'	Exchange the contents of BC, DE, HL with contents of BC', DE', HL', respectively	1	4	•	•	•	•	•	•	11 011 001
HALT	Processor Halted	HALT (wait for interrupt or reset)	1	4	•	•	•	•	•	•	01 110 110
IM 0		Set Interrupt mode 0	2	8	•	•	•	•	•	•	11 101 101 01 000 110
IM 1		Set Interrupt mode 1	2	8	•	•	•	•	•	•	11 101 101 01 010 110
IM 2		Set Interrupt mode 2	2	8	•	•	•	•	•	•	11 101 101 01 011 110
IN A, (n)	A ← (n)	Load ACC with input from device n	2	11	•	•	•	•	•	•	11 011 011 nn nnn nnn
IN r, (C)	r ← (C)	Load Reg. r with input from device (C)	2	12	•	↕	P	↕	0	↕	11 101 101① 01 rrr 000
INC (HL)	(HL) ← (HL) + 1	Increment location (HL)	1	11	•	↕	V	↕	0	↕	00 110 100
INC IX	IX ← IX + 1	Increment IX	2	10	•	•	•	•	•	•	11 011 101 00 100 011
INC (IX + d)	(IX + d) ← (IX + d) + 1	Increment location (IX + d)	3	23	•	↕	V	↕	0	↕	11 011 101 00 110 100 dd ddd ddd
INC IY	IY ← IY + 1	Increment IY	2	10	•	•	•	•	•	•	11 111 101 00 100 011
INC (IY + d)	(IY + d) ← (IY + d) + 1	Increment location (IY + d)	3	23	•	↕	V	↕	0	↕	11 111 101 00 110 100 dd ddd ddd
INC r	r ← r + 1	Increment Reg. r	1	4	•	↕	V	↕	0	↕	00 rrr 100Ⓑ
INC ss	ss ← ss + 1	Increment Reg. pair ss	1	6	•	•	•	•	•	•	00 ss0 011Ⓐ
IND	(HL) ← (C) B ← B – 1 HL ← HL – 1	Load location (HL) with input from port (C), decrement HL and B	2	16	•	↕③	X	X	1	X	11 101 101 10 101 010

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
INDR	(HL) ← (C) B ← B – 1 HL ← HL – 1 until B = 0	Load location (HL) with input from port (C), decrement HL and decrement B, repeat until B = 0	2	21	•	1	X	X	1	X	11 101 101 10 111 010
INI	(HL) ← (C) B ← B – 1 HL ← HL + 1	Load location (HL) with input from port (C); and increment HL and decrement B	2	16	•	↕③	X	X	1	X	11 101 101 10 100 010
INIR	(HL) ← (C) B ← B – 1 HL ← HL + 1 until B = 0	Load location (HL) with input from port (C), increment HL and decrement B, repeat until B = 0	2	21	•	1	X	X	1	X	11 101 101 10 110 010
JP (HL)	PC ← HL	Unconditional jump to (HL)	1	4	•	•	•	•	•	•	11 101 001
JP (IX)	PC ← IX	Unconditional jump to (IX)	2	8	•	•	•	•	•	•	11 011 101 11 101 001
JP (IY)	PC ← IY	Unconditional jump to (IY)	2	8	•	•	•	•	•	•	11 111 101 11 101 001
JP cc, nn	If cc true PC ← nn else continue	Jump to location nn if condition cc is true	3	10	•	•	•	•	•	•	11 ←cc→ 010Ⓗ nn nnn nnn nn nnn nnn
JP nn	PC ← nn	Unconditional jump to location nn	3	10	•	•	•	•	•	•	11 000 011 nn nnn nnn nn nnn nnn
JR C, e	If C = 0 continue If C = 1 PC ← PC + e	Jump relative to PC + e, if carry = 1	2	7 if condition met. 12, if not	•	•	•	•	•	•	00 111 000 ←e-2→
JR e	PC ← PC + e	Unconditional jump relative to PC + e	2	12	•	•	•	•	•	•	00 011 000 ←e-2→
JR NC, e	If C = 1 continue If C = 0 PC ← PC + e	Jump relative to PC + e if carry = 0	2	7	•	•	•	•	•	•	00 110 000 ←e-2→
JR NZ, e	If Z = 1 continue	Jump relative to PC + e if non-zero (Z = 0)	2	7	•	•	•	•	•	•	00 100 000 ←e-2→
JR Z, e	If Z = 0 continue	Jump relative to PC + e if zero (Z = 1)	2	7	•	•	•	•	•	•	00 101 000 ←e-2→
LD A, (BC)	A ← (BC)	Load ACC with location (BC)	1	7	•	•	•	•	•	•	00 001 010
LD A, (DE)	A ← (DE)	Load ACC with location (DE)	1	7	•	•	•	•	•	•	00 011 010
LD A, I	A ← I	Load ACC with I	2	9	•	↕	IFF	↕	0	0	11 101 101 01 010 111
LD A, (nn)	A ← (nn)	Load ACC with location nn	3	13	•	•	•	•	•	•	00 111 010 nn nnn nnn nn nnn nnn
LD A, R	A ← R	Load ACC with Reg. R	2	9	•	↕	IFF	↕	0	0	11 101 101 01 011 111
LD (BC), A	(BC) ← A	Load location (BC) with ACC	1	7	•	•	•	•	•	•	00 000 010
LD (DE), A	(DE) ← A	Load location (DE) with ACC	1	7	•	•	•	•	•	•	00 010 010
LD (HL), n	(HL) ← n	Load location (HL) with value n	2	10	•	•	•	•	•	•	00 110 110 nn nnn nnn
LD ss, nn	ss ← nn	Load Reg. pair ss with value nn	4	20	•	•	•	•	•	•	00 ss0 001Ⓐ nn nnn nnn nn nnn nnn
LD HL, (nn)	H ← (nn + 1) L ← (nn)	Load HL with location (nn)	3	16	•	•	•	•	•	•	00 101 010 nn nnn nnn nn nnn nnn
LD (HL), r	(HL) ← r	Load location (HL) with Reg. r	1	7	•	•	•	•	•	•	01 110 r r rⒷ
LD I, A	I ← A	Load I with ACC	2	9	•	•	•	•	•	•	11 101 101 01 000 111
LD IX, nn	IX ← nn	Load IX with value nn	4	19	•	•	•	•	•	•	11 011 101 00 100 001 nn nnn nnn nn nnn nnn
LD IX, (nn)	IX_H ← (nn + 1) IX_L ← (nn)	Load IX with location (nn)	4	20	•	•	•	•	•	•	11 011 101 00 101 010 nn nnn nnn nn nnn nnn
LD (IX + d), n	(IX + d) ← n	Load location (IX + d) with value n	4	19	•	•	•	•	•	•	11 011 101 00 110 110 dd ddd ddd nn nnn nnn
LD (IX + d), r	(IX + d) ← r	Load location (IX + d) with Reg. r	3	19	•	•	•	•	•	•	11 011 101Ⓑ 01 110 r r r dd ddd ddd

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
LD IY, nn	IY ← nn	Load IY with value nn	4	14	•	•	•	•	•	•	11 111 101 00 100 001 nn nnn nnn nn nnn nnn
LD IY, (nn)	IY_H ← (nn + 1) IY_L ← (nn)	Load IY with location (nn)	4	20	•	•	•	•	•	•	11 111 101 00 101 010 nn nnn nnn nn nnn nnn
LD ss, (nn)	ss_H ← (nn + 1) ss_L ← (nn)	Load Reg. pair dd with location (nn)	4	20	•	•	•	•	•	•	11 101 101 Ⓐ 01 ss1 011 nn nnn nnn nn nnn nnn
LD (IY + d), n	(IY + d) ← n	Load (IY + d) with value n	4	19	•	•	•	•	•	•	11 111 101 00 110 110 dd ddd ddd nn nnn nnn
LD (IY + d), r	(IY + d) ← r	Load location (IY + d) with Reg. r	3	19	•	•	•	•	•	•	11 111 101 Ⓑ 01 110 rrr dd ddd ddd
LD (nn), A	(nn) ← A	Load location (nn) with ACC	3	13	•	•	•	•	•	•	00 110 010 nn nnn nnn nn nnn nnn
LD (nn), ss	(nn + 1) ← ss_H (nn) ← ss_L	Load location (nn) with Reg. pair dd	4	20	•	•	•	•	•	•	11 101 101 Ⓐ 01 ss0 011 nn nnn nnn nn nnn nnn
LD (nn), HL	(nn + 1) ← H (nn) ← L	Load location (nn) with HL	3	16	•	•	•	•	•	•	00 100 010 nn nnn nnn nn nnn nnn
LD (nn), IX	(nn + 1) ← IX_H (nn) ← IX_L	Load location (nn) with IX	4	20	•	•	•	•	•	•	11 011 101 00 100 010 nn nnn nnn nn nnn nnn
LD (nn), IY	(nn + 1) ← IY_H (nn) ← IY_L	Load location (nn) with IY	4	20	•	•	•	•	•	•	11 111 101 00 100 010 nn nnn nnn nn nnn nnn
LD R, A	R ← A	Load R with ACC	2	9	•	•	•	•	•	•	11 101 101 01 001 111
LD r, (HL)	r ← (HL)	Load Reg. r with location (HL)	1	7	•	•	•	•	•	•	01 rrr 110 Ⓑ
LD r, (IX + d)	r ← (IX + d)	Load Reg. r with location (IX + d)	3	19	•	•	•	•	•	•	11 011 101 Ⓑ 01 rrr 110 dd ddd ddd
LD r, (IY + d)	r ← (IY + d)	Load Reg. r with location (IY + d)	3	19	•	•	•	•	•	•	11 111 101 Ⓑ 01 rrr 110 dd ddd ddd
LD r, n	r ← n	Load Reg. r with value n	2	7	•	•	•	•	•	•	00 rrr 110 Ⓑ nn nnn nnn
LD, r, r'	r ← r'	Load Reg. r with Reg. r	1	4	•	•	•	•	•	•	01 rrr r'r'r' Ⓕ
LD SP, HL	SP ← HL	Load SP with HL	1	6	•	•	•	•	•	•	11 111 001
LD SP, IX	SP ← IX	Load SP with IX	2	10	•	•	•	•	•	•	11 011 101 11 111 001
LD SP, IY	SP ← IY	Load SP with IY	2	10	•	•	•	•	•	•	11 111 101 11 111 001
LDD	(DE) ← (HL) DE ← DE − 1 HL ← HL − 1 BC ← BC − 1	Load location (DE) with location (HL), decrement DE, HL and BC	2	16	•	•	↕	•	0	0	11 101 101 10 101 000
LDDR	(DE) ← (HL) DE ← DE − 1 HL ← HL − 1 BC ← BC − 1 until BC = 0	Load location (DE) with location (HL)	2	21	•	•	0	•	0	0	11 101 101 10 111 000
LDI	(DE) ← (HL) DE ← DE + 1 HL ← HL + 1 BC ← BC − 1	Load location (DE) with location (HL), increment DE, HL; decrement BC	2	16	•	•	↕①	•	0	0	11 101 101 10 100 000
LDIR	(DE) ← (HL) DE ← DE + 1 HL ← HL + 1 BC ← BC − 1 until BC = 0	Load location (DE) with location (HL), increment DE, HL; decrement BC and repeat until BC = 0	2	21 if BC ≠ 0 16 if BC = 0	•	•	0	•	0	0	11 101 101 10 110 000
NEG	A ← 0 − A	Negate ACC (2's complement)	2	8	↕	↕	V	↕	1	↕	11 101 101 01 000 100

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
NOP		No operation	1	4	•	•	•	•	•	•	00 000 000
OR r	A ← AV r	Logical 'OR' of Reg. r and ACC		4	0	↕	P	↕	0	↕	10 110 rrr Ⓑ
OR n	A ← AV n	Logical 'OR' of value n and ACC		7	•	↕	P	↕	0	↕	11 110 110 nn nnn nnn
OR (HL)	A ← AV (HL)	Logical 'OR' of loc. (HL) and ACC		7	•	↕	P	↕	0	↕	10 110 110
OR (IX + d)	A ← (IX + d)	Logical 'OR' of loc. (IX + d) ∧ ACC		19	•	↕	P	↕	0	↕	11 011 101 10 110 110 dd ddd ddd
OR (IY + d)	A ← AV (IY + d)	Logical 'OR' of loc. (IY + d) ∧ ACC		19	•	↕	P	↕	0	↕	11 111 101 10 110 110 dd ddd ddd
OTDR	(C) ← (HL) B ← B − 1 HL ← HL − 1 until B = 0	Load output port (C) with contents of location (HL), decrement HL and B, repeat until B = 0	2	21 if B ≠ 0 16 if B = C	•	1	X	X	1	X	11 101 101 10 111 011
OTIR	(C) ← (HL) B ← B − 1 HL ← HL + 1 until B = 0	Load output port (C) with location (HL), increment HL, decrement B, repeat until B = 0	2	21 if B ≠ 0 16 if B = C	•	1	X	X	1	X	11 101 101 10 110 011
OUT (C), r	(C) ← r	Load output port (C) with Reg. r	2	12	•	•	•	•	•	•	11 101 101 Ⓑ 01 rrr 001
OUT (n), A	(n) ← A	Load output port (n) with ACC	2	11	•	•	•	•	•	•	11 010 011 nn nnn nnn
OUTD	(C) ← (HL) B ← B − 1 HL ← HL − 1	Load output port (C) with location (HL), increment HL and decrement B	2	16	•	↕③	X	X	1	X	11 101 101 10 101 011
OUTI	(C) ← (HL) B ← B − 1 HL ← HL + 1	Load output port (C) with location (HL), increment HL and decrement B	2	16	•	↕③	X	X	1	X	11 101 101 10 100 011
POP IX	IX_H ← (SP + 1) IX_L ← (SP)	Load IX with top of stack	2	14	•	•	•	•	•	•	11 011 101 11 100 001
POP IY	IY_H ← (SP + 1) IY_L ← (SP)	Load IY with top of stack	2	14	•	•	•	•	•	•	11 111 101 11 100 001
POP qq	qq_H ← (SP + 1) qq_L ← (SP)	Load Reg. pair qq with top of stack	1	10	•	•	•	•	•	•	11 qq0 001 Ⓖ
PUSH IX	(SP − 2) ← IX_L (SP − 1) ← IX_H	Load IX onto stack	2	15	•	•	•	•	•	•	11 011 101 11 100 101
PUSH IY	(SP − 2) ← IY_L (SP − 1) ← IY_H	Load IY onto stack	2	15	•	•	•	•	•	•	11 111 101 11 100 101
PUSH qq	(SP − 2) ← qq_L (SP − 1) ← qq_H	Load Reg. pair qq onto stack	1	11	•	•	•	•	•	•	11 qq0 101 Ⓖ
RES b, r	S_b ← 0	Reset Bit b of Reg. r		8	•	•	•	•	•	•	11 001 011 Ⓑ 10 bbb rrr Ⓔ
RES b, (HL)	S_b ← 0, (HL)	Reset Bit b of loc. (HL)		15	•	•	•	•	•	•	11 001 011 10 bbb 110
RES b, (IX + d)	S_b ← 0, (IX + d)	Reset Bit b of loc. (IX + d)		23	•	•	•	•	•	•	11 011 101 11 001 011 dd ddd ddd 10 bbb 110
RES b, (IY + d)	S_b ← 0, (IY + d)	Reset Bit b of loc. (IY + d)		23	•	•	•	•	•	•	11 111 101 11 001 011 dd ddd ddd 10 bbb 110
RET	PC_L ← (SP) PC_H ← (SP + 1)	Return from subroutine	1	10	•	•	•	•	•	•	11 001 001
RET cc	If condition cc is false cont. else (PC_L ← (SP) PC_H ← (SP + 1)	Return from subroutine if condition cc is true	1	5 if CC false 11 if CC true	•	•	•	•	•	•	11 ←cc→ 000 Ⓗ
RETI		Return from interrupt	2	14	•	•	•	•	•	•	11 101 101 01 001 101
RETN		Return from non-maskable interrupt	2	14	•	•	•	•	•	•	11 101 101 01 000 101
RL r		Rotate left through carry Reg. r		2	↕	↕	P	↕	0	0	11 001 011 Ⓑ 00 010 rrr
RL (HL)		Rotate left through carry loc. (HL)		4	↕	↕	P	↕	0	0	11 001 011 00 010 110
RL (IX + d)		Rotate left through carry loc. (IX + d)		6	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 010 110
RL (IY + d)	m ≅ r, (HL), (IX + d), (IY + d), A	Rotate left through carry loc. (IY + d)		6	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 010 110
RLA		Rotate left ACC through carry	1	4	↕	•	•	•	0	0	00 010 111

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
RLC (HL)		Rotate location (HL) left circular	2	15	↕	↕	P	↕	0	0	11 001 011 00 000 110
RLC (IX + d)		Rotate location (IX + d) left circular	4	23	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 000 110
RLC (IY + d)	 m ≡ r, (HL), (IX + d), (IY + d), A	Rotate location (IY + d) left circular	4	23	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 000 110
RLC r		Rotate Reg. r left circular	2	8	↕	↕	P	↕	0	0	11 001 011 (B) 00 000 r r r
RLCA		Rotate left circular ACC	1	4	↕	•	•	•	0	0	00 000 111
RLD		Rotate digit left and right between ACC and location (HL)	2	18	•	↕	P	↕	0	0	11 101 101 01 101 111
RR r		Rotate right through carry Reg. r		2	↕	↕	P	↕	0	0	11 001 011 (B) 00 011 r r r
RR (HL)		Rotate right through carry loc. (HL)		4	↕	↕	P	↕	0	0	11 001 011 00 011 110
RR (IX + d)		Rotate right through carry loc. (IX + d)		6	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 011 110
RR (IY + d)	 m ≡ r, (HL), (IX + d), (IY + d), A	Rotate right through carry loc. (IY + d)		6	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 011 110
RRA		Rotate right ACC through carry	1	4	↕	•	•	•	0	0	00 011 111
RRC r		Rotate Reg. r right circular		2	↕	↕	P	↕	0	0	11 001 011 (B) 00 001 r r r
RRC (HL)		Rotate loc. (HL) right circular		4	↕	↕	P	↕	0	0	11 001 011 00 001 110
RRC (IX + d)		Rotate loc. (IX + d) right circular		6	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 001 110
RRC (IY + d)	m ≡ r, (HL), (IX + d), (IY + d), A	Rotate loc. (IY + d) right circular		6	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 001 110
RRCA		Rotate right circular ACC	1	4	↕	•	•	•	0	0	00 001 111
RRD		Rotate digit right and left between ACC and location (HL)	2	18	•	↕	P	↕	0	0	11 101 101 01 100 111
RST_t	(SP − 1) ← PC_H (SP − 2) ← PC_L PC_H ← 0, PC_L ← T	Restart to location T	1	11	•	•	•	•	•	•	11 t t t 111
SBC A, r	A ← A − r − CY	Subtract Reg. r from ACC w/carry	1	4	↕	↕	V	↕	1	↕	10 011 r r r (B)
SBC A, n	A ← A − n − CY	Subtract value n from ACC with carry		7	↕	↕	V	↕	1	↕	11 011 110 n n n n n n n n
SBC A, (HL)	A ← A − (HL) − CY	Sub. loc. (HL) from ACC w/carry		7	↕	↕	V	↕	1	↕	10 011 110
SBC A, (IX + d)	A ← A − (IX + d) − CY	Subtract loc. (IX + d) from ACC with carry		19	↕	↕	V	↕	1	↕	11 011 101 10 011 110 dd ddd ddd
SBC A, (IY + d)	A ← A − (IY + d) − CY	Subtract loc. (IY + d) from ACC with carry		19	↕	↕	V	↕	1	↕	11 111 101 10 011 110 dd ddd ddd
SBC HL, ss	HL ← HL − ss − CY	Subtract Reg. pair ss from HL with carry	2	15	↕	↕	V	↕	1	X	11 101 101 (A) 01 s s 0 010
SCF	CY ← 1	Set carry flag (C = 1)	1	4	1	•	•	•	0	0	00 110 111
SET b, (HL)	$(HL)_b$ ← 1	Set Bit b of location (HL)	2	15	•	•	•	•	•	•	11 001 011 (E) 11 b b b 110
SET b, (IX + d)	$(IX + d)_b$ ← 1	Set Bit b of location (IX + d)	4	23	•	•	•	•	•	•	11 011 101 (E) 11 001 011 dd ddd ddd 11 b b b 110

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
SET b, (IY + d)	$(IY + d)_b \leftarrow 1$	Set Bit b of location (IY + d)	4	23	•	•	•	•	•	•	11 111 101 Ⓔ 11 001 011 dd ddd ddd 11 bbb 110
SET b, r	$r_b \leftarrow 1$	Set Bit b of Reg. r	2	8	•	•	•	•	•	•	11 001 011 Ⓑ 11 bbb rrr
SLA r		Shift Reg. r left arithmetic		8	↕	↕	P	↕	0	0	11 001 011 Ⓑ 00 100 rrr
SLA (HL)		Shift loc. (HL) left arithmetic		15	↕	↕	P	↕	0	0	11 001 011 00 100 110
SLA (IX + d)		Shift loc. (IX + d) left arithmetic		23	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 100 110
	m ≡ r, (HL), (IX + d), (IY + d)										
SLA (IY + d)		Shift loc. (IY + d) left arithmetic		23	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 100 110
SRA r		Shift Reg. r right arithmetic		8	↕	↕	P	↕	0	0	11 001 011 Ⓑ 00 101 rrr
SRA (HL)		Shift loc. (HL) right arithmetic		15	↕	↕	P	↕	0	0	11 001 011 00 101 110
SRA (IX + d)		Shift loc. (IX + d) right arithmetic		23	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 101 110
	m ≡ r, (HL), (IX + d), (IY + d)										
SRA (IY + d)		Shift loc. (IY + d) right arithmetic		23	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 101 110
SRL r		Shift Reg. r right logical		8	↕	↕	P	↕	0	0	11 001 011 Ⓑ 00 111 rrr
SRL (HL)		Shift loc. (HL) right logical		15	↕	↕	P	↕	0	0	11 001 011 00 111 110
SRL (IX + d)		Shift loc. (IX + d) right logical		23	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 111 110
	m ≡ r, (HL), (IX + d), (IY + d)										
SRL (IY + d)		Shift loc. (IY + d) right logical		23	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 111 110
SUB r	A ← A - r	Subtract Reg. r from ACC		4	↕	↕	V	↕	1	↕	10 010 rrr Ⓑ
SUB n	A ← A - n	Subtract value n from ACC		7	↕	↕	V	↕	1	↕	11 010 110 nn nnn nnn
SUB (HL)	A ← A - (HL)	Subtract loc. (HL) from ACC		7	↕	↕	V	↕	1	↕	10 010 110
SUB (IX + d)	A ← A - (IX + d)	Subtract loc. (IX + d) from ACC		19	↕	↕	V	↕	1	↕	11 011 101 10 010 110 dd ddd ddd
SUB (IY + d)	A ← A - (IY + d)	Subtract loc. (IY + d) from ACC		19	↕	↕	V	↕	1	↕	11 111 101 10 010 110 dd ddd ddd
XOR r	A ← A∀r	Exclusive 'OR' Reg. r and ACC		4	↕	↕	P	↕	1	↕	10 101 rrr Ⓑ
XOR n	A ← A∀n	Exclusive 'OR' value n and ACC		7	↕	↕	P	↕	1	↕	11 101 110 nn nnn nnn
XOR (HL)	A ← A∀ (HL)	Exclusive 'OR' loc. (HL) and ACC		7	↕	↕	P	↕	1	↕	10 101 110
XOR (IX + d)	A ← A∀ (IX + d)	Exclusive 'OR' loc. (IX + d) and ACC		19	↕	↕	P	↕	1	↕	11 011 101 10 101 110 dd ddd ddd
XOR (IY + d)	A ← A∀ (IY + d)	Exclusive 'OR' loc. (IY + d) and ACC		19	↕	↕	P	↕	1	↕	11 111 101 10 101 110 dd ddd ddd

FLAG NOTES:

① P/V flag is 0 if B-1=0, else P/V=1

② Z=1 if A=(HL), else Z=0

③ If B-1=0, Z flag set, else reset

FLAG DEFINITIONS

• = Flag not affected

0 = Flag reset

1 = Flag set

X = Flag unknown

↕ = Flag affected according to result of operation

V = Overflow set

P = Parity set

IFF = Interrupt flip-flop set

Ⓐ

Reg	ss
BC	00
DE	01
HL	10
SP	11

Ⓑ

Reg	r
A	111
B	000
C	001
D	010
E	011
H	100
L	101

Ⓒ

Reg	pp
BC	00
DE	01
IX	10
SP	11

Ⓓ

Reg	rr
BC	00
DE	01
IY	10
SP	11

Ⓔ

Bit	b
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

Ⓕ

Reg	r,r'
A	111
B	000
C	001
D	010
E	011
H	100
L	101

Ⓖ

Reg	qq
BC	00
DE	01
HL	10
AF	11

Ⓗ

CC	Condition		Relevant Flag
000	NZ	Non Zero	Z
001	Z	Zero	Z
010	NC	Non Carry	C
011	C	Carry	C
100	PO	Parity Odd	P/V
101	PE	Parity Even	P/V
110	P	Sign Positive	S
111	M	Sign Negative	S

Ⓘ

Reg	r
B	000
C	001
D	010
E	011
H	100
L	101
F	110
A	111

FLAG DESCRIPTION:

C = Carry/Link
Z = Zero
P/V = Parity/Overflow
S = Sign
N = Add/Subtract
H = Half Carry

The information presented in this document is believed to be accurate and reliable. The information is subject to change without notice.

PROGRAMMABLE COMMUNICATION INTERFACE

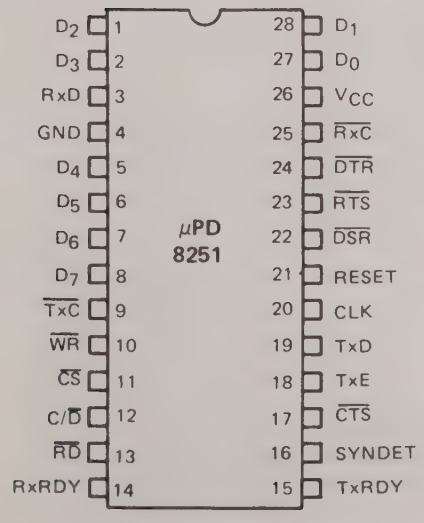
DESCRIPTION

The μPD8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is designed for microcomputer systems data communications. The USART is used as a peripheral and is programmed by the μPD8080 or other processor to communicate in commonly used serial data transmission techniques including IBM Bi-Sync. The USART receives serial data streams and converts them into parallel data characters for the processor. While receiving serial data, the USART will also accept data characters from the processor in parallel format, convert them to serial format and transmit. The USART will signal the processor when it has completely received or transmitted a character and requires service. Complete USART STATUS including data format errors and control signals such as TxE and SYNDET is available to the processor at any time.

FEATURES

- Asynchronous or Synchronous Operation
  - Asynchronous:
    - 5-8 Bit Characters
    - Clock Rate – 1, 16 or 64 x Baud Rate
    - Break Character Generation
    - Select 1, 1-1/2, or 2 Stop Bits
    - False Start Bit Detector
  - Synchronous:
    - 5-8 Bit Characters
    - Internal or External Character Synchronization
    - Automatic Sync Insertion
    - Single or Double Sync Characters
- Baud Rate – Synchronous – DC to 56K Baud
  – Asynchronous – DC to 9.6K Baud
- Full Duplex, Double Buffered Transmitter and Receiver
- Parity, Overrun and Framing Flags
- Fully Compatible with 8080
- All Inputs and Outputs are TTL Compatible
- Single +5 Volt Supply
- Separate Device, Receive and Transmit TTL Clocks
- 28 Pin Plastic DIP Package
- N-Channel MOS Technology

PIN CONFIGURATION



PIN NAMES

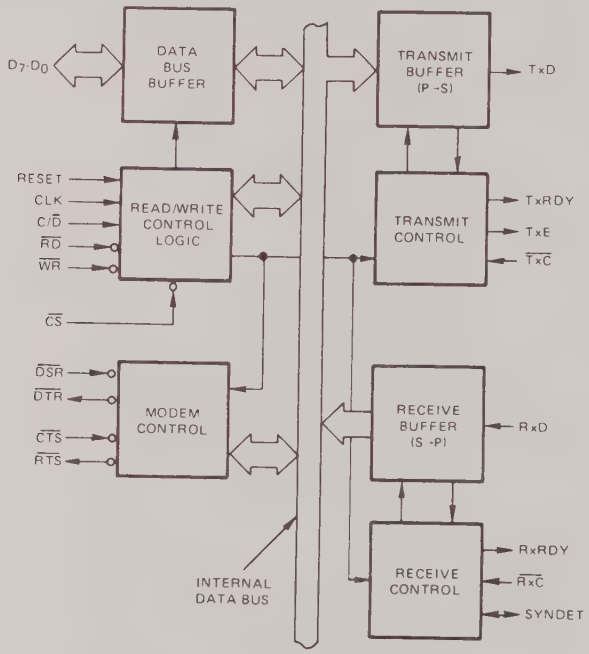
D_7-D_0	Data Bus (8 bits)
C/D	Control or Data is to be Written or Read
RD	Read Data Command
WR	Write Data or Control Command
CS	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
TxC	Transmitter Clock (TTL)
TxD	Transmitter Data
RxC	Receiver Clock (TTL)
RxD	Receiver Data
RxRDY	Receiver Ready (has character for 8080)
TxRDY	Transmitter Ready (ready for char. from 8080)
DSR	Data Set Ready
DTR	Data Terminal Ready
SYNDET	Sync Detect
RTS	Request to Send Data
CTS	Clear to Send Data
TxE	Transmitter Empty
V_{CC}	+5 Volt Supply
GND	Ground

FUNCTIONAL DESCRIPTION

The μPD8251 Universal Synchronous/Asynchronous Receiver/Transmitter is designed specifically for 8080 microcomputer systems but works with most 8-bit processors. Operation of the 8251, like other I/O devices in the 8080 family, is programmed by system software for maximum flexibility.

In the receive mode, a communication interface device must convert incoming serial format data into parallel data and make certain format checks on the data. And in the transmit mode, the device must format data into serial data. The device must also supply or remove characters or bits that are unique to the communication format in use. By performing conversion and formatting services automatically, the USART appears to the processor as a simple or "transparent" input or output of byte-oriented parallel data.

BLOCK DIAGRAM



BASIC OPERATION

C/D	RD	WR	CS	
0	0	1	0	8251 → Data Bus
0	1	0	0	Data Bus → 8251
1	0	1	0	Status → Data Bus
1	1	0	0	Data Bus → Control
X	X	X	1	Data Bus → 3-State
X	1	1	0	

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . -0°C to +70°C
Storage Temperature . . . . . -65°C to +125°C
All Output Voltages . . . . . -0.5 to +7 Volts
All Input Voltages . . . . . -0.5 to +7 Volts
Supply Voltages . . . . . -0.5 to +7 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

$T_a = 0°C$ to $70°C$; $V_{CC} = 5.0V \pm 5\%$; GND = 0V

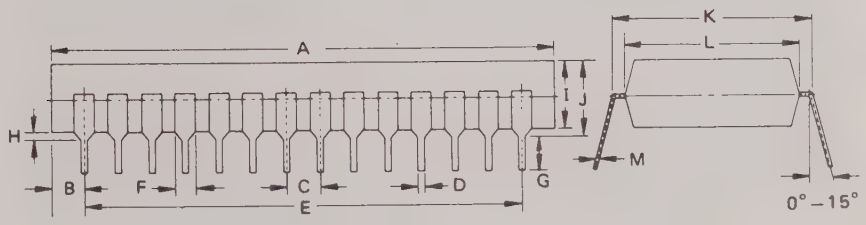
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	GND −.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC}	V	
Output Low Voltage	V_{OL}			0.45	V	$I_{OL} = 1.7$ mA
Output High Voltage	V_{OH}	2.4			V	$I_{OH} = -100\ \mu A$
Data Bus Leakage	I_{DL}			−50	μA	$V_{OUT} = 0.45V$
				10	μA	$V_{OUT} = V_{CC}$
Input Load Current	I_{IL}			10	μA	@5.5V
Power Supply Current	I_{CC}		45	80	mA	

CAPACITANCE

$T_a = 25°C$; V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	fc = 1 MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to GND

PACKAGE OUTLINE μPD8251C



ITEM	MILLIMETERS	INCHES
A	38.0 MAX.	1.496 MAX.
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

BUS PARAMETERS: ①

T_a = 0°C to 70°C; V_{CC} = 5.0V ± 5%; GND = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
READ						
Address Stable before $\overline{READ}$, ($\overline{CS}$, C/$\overline{D}$)	t_{AR}	50			ns	
Address Hold Time for $\overline{READ}$, ($\overline{CS}$, $\overline{CD}$)	t_{RA}	5			ns	
$\overline{READ}$ Pulse Width	t_{RR}	430			ns	
Data Delay from $\overline{READ}$	t_{RD}			350	ns	C_L = 100 pF
$\overline{READ}$ to Data Floating	t_{DF}	25		200	ns	C_L = 100 pF C_L = 15 pF
Recovery Time Between WRITES ②	t_{RV}	6			t_{CY}	
WRITE						
Address Stable before $\overline{WRITE}$	t_{AW}	20			ns	
Address Hold Time for $\overline{WRITE}$	t_{WA}	20			ns	
$\overline{WRITE}$ Pulse Width	t_{WW}	400			ns	
Data Set-Up Time for $\overline{WRITE}$	t_{DW}	200			ns	
Data Hold Time for $\overline{WRITE}$	t_{WD}	40			ns	
OTHER TIMING						
Clock Period ③	t_{CY}	.420		1.35	µs	
Clock Pulse Width	$t_{\Phi W}$	220		0.7t_{CY}	ns	
Clock Rise and Fall Time	t_{R},t_F	0		50	ns	
TxD Delay from Falling Edge of TxC	t_{DTx}			1	µs	C_L = 100 pF
Rx Data Set-Up Time to Sampling Pulse	$t_{SR\#}$	2			µs	C_L = 100 pF
Rx Data Hold Time to Sampling Pulse	t_{HRx}	2			µs	C_L = 100 pF
Transmitter Input Clock Frequency 1X Baud Rate 16X and 64X Baud Rate	$f_{T\#}$	DC DC		56 520	KHz KHz	
Transmitter Input Clock Pulse Width 1X Baud Rate 16X and 64X Baud Rate	t_{TPW}	12 1			t_{CY} t_{CY}	
Transmitter Input Clock Pulse Delay 1X Baud Rate 16X and 64X Baud Rate	t_{TPD}	15 3			t_{CY} t_{CY}	
Receiver Input Clock Frequency 1X Baud Rate 16X and 64X Baud Rate	f_{Rx}	DC DC		56 520	KHz KHz	
Receiver Input Clock Pulse Width 1X Baud Rate 16X and 64X Baud Rate	t_{RPW}	12 1			t_{CY} t_{CY}	
Receiver Input Clock Pulse Delay 1X Baud Rate 16X and 64X Baud Rate	t_{RPD}	15 3			t_{CY} t_{CY}	
TxRDY Delay from Center of Data Bit	$t_{T\#}$			16	t_{CY}	C_L = 50 pF
RxRDY Delay from Center of Data Bit	t_{Rx}			20	t_{CY}	
Internal Syndet Delay from Center of Data Bit	t_{IS}			25	t_{CY}	
External Syndet Set-Up Time before Falling Edge of $\overline{RxC}$	t_{ES}	16		16	t_{CY}	
TxEMPTY Delay from Center of Data Bit	t_{TxE}			16	t_{CY}	C_L = 50 pF
Control Delay from Rising Edge of WRITE (TxE, $\overline{DTR}$, $\overline{RTS}$)	t_{WC}				t_{CY}	
Control to READ Set-Up Time ($\overline{DSR}$, $\overline{CTS}$)	t_{CR}	16			t_{CY}	

Notes ① AC timings measured at V_{OH} = 2.0, V_{OL} = 0.3, and with load circuit of Figure 1.

② This recovery time is for initialization only, when MODE, SYNC1, SYNC2, COMMAND and first DATA BYTES are written into the USART. Subsequent writing of both COMMAND and DATA are only allowed when TxRDY = 1.

③ The TxC and RxC frequencies have the following limitations with respect to CLK.
For 1X Baud Rate, f_{Tx} or $f_{Rx} \leq 1/(30\ t_{CY})$
For 16X and 64X Baud Rate, f_{Tx} or $f_{Rx} \leq 1/(4.5\ t_{CY})$

④ Reset Pulse Width = 6 t_{CY} minimum.

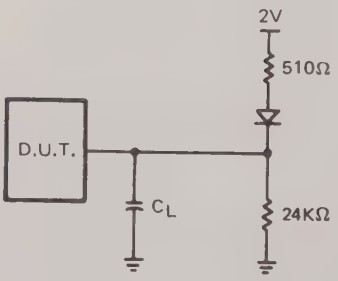
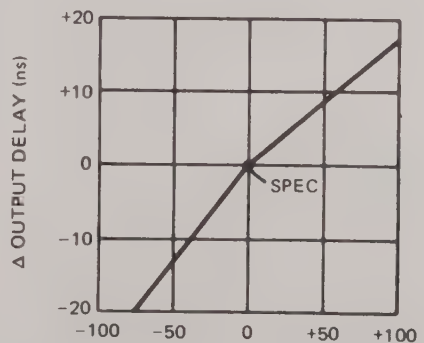


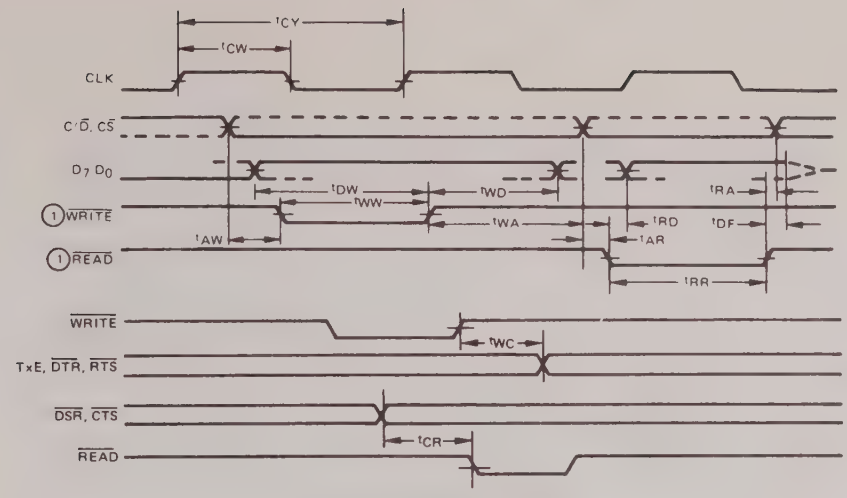
Figure 1.

TEST LOAD CIRCUIT

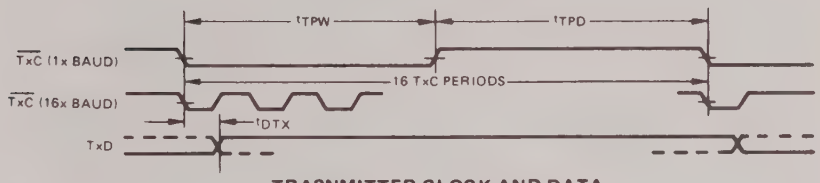


Typical Δ Output Delay Versus Δ Capacitance (pF)

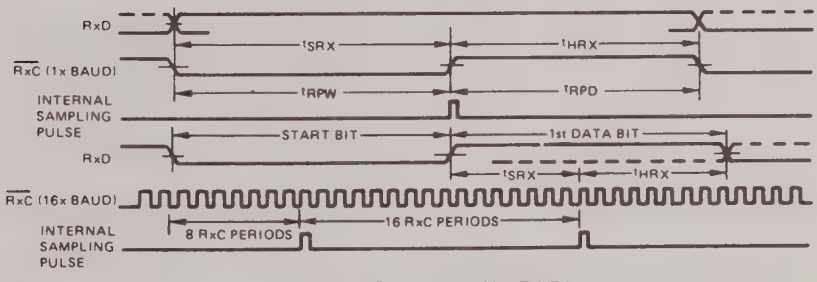
TIMING WAVEFORMS



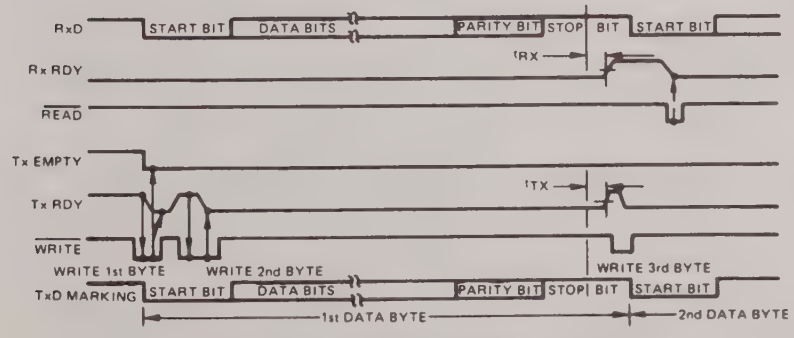
READ AND WRITE TIMING



TRASNMITTER CLOCK AND DATA

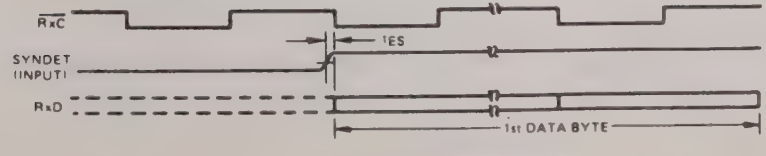


RECEIVER CLOCK AND DATA



TxRDY AND RxRDY TIMING (ASYNC MODE)

INTERNAL SYNC DETECT



EXTERNAL SYNC DETECT

Note: (1) Write and Read pulses have no timing limitation with respect to CLK.

PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
1, 2, 27, 28 5 – 8	$D_7 - D_0$	Data Bus Buffer	An 8-bit, 3-state bi-directional buffer used to interface the 8251 to the processor data bus. Data is transmitted or received by the buffer in response to input/output or Read/Write instructions from the processor. The Data Bus Buffer also transfers Control words, Command words, and Status.
26	V_{CC}	V_{CC} Supply Voltage	+5 volt supply
4	GND	Ground	Ground
Read/Write Control Logic			This logic block accepts inputs from the processor Control Bus and generates control signals for overall USART operation. The Mode Instruction and Command Instruction registers that store the control formats for device functional definition are located in the Read/ Write Control Logic.
21	RESET	Reset	A "one" on this input forces the USART into the "Idle" mode where it will remain until reinitialized with a new set of control words. Minimum RESET pulse width is t_{CY}.
20	CLK	Clock Pulse	The CLK input provides for internal device timing and is usually connected to the Phase 2 (TTL) output of the μPB8224 Clock Generator. External inputs and outputs are not referenced to CLK, but the CLK frequency must be 30 times the Receiver or Transmitter clocks in the synchronous mode and 4.5 times for the asynchronous mode.
10	$\overline{WR}$	Write Data	A "zero" on this input instructs the μPD8251 to accept the data or control word which the processor is writing out to the USART via the data bus.
13	$\overline{RD}$	Read Data	A "zero" on this input instructs the μPD8251 to place the data or status information onto the Data Bus for the processor to read.
12	C/$\overline{D}$	Control/Data	The Control/Data input, in conjunction with the $\overline{WR}$ and $\overline{RD}$ inputs, informs USART to accept or provide either a data character, control word or status information via the Data Bus. 0 = Data; 1 = Control.
11	$\overline{CS}$	Chip Select	A "zero" on this input enables the USART for reading and writing to the processor.
Modem Control			The μPD8251 has a set of control inputs and outputs which may be used to simplify the interface to a Modem.
22	$\overline{DSR}$	Data Set Ready	The Data Set Ready input can be tested by the processor via Status information. The $\overline{DSR}$ input is normally used to test Modem Data Set Ready condition.
24	$\overline{DTR}$	Data Terminal Ready	The Data Terminal Ready output can be controlled via the Command word. The $\overline{DTR}$ output is normally used to drive Modem Data Terminal Ready or Rate Select lines.
23	$\overline{RTS}$	Request to Send	The Request to Send output can be controlled via the Command word. The $\overline{RTS}$ output is normally used to drive the Modem Request to Send line.
17	$\overline{CTS}$	Clear to Send	A "zero" on the Clear to Send input enables the USART to transmit serial data if the TxEN bit in the Command Instruction register is enabled (one).

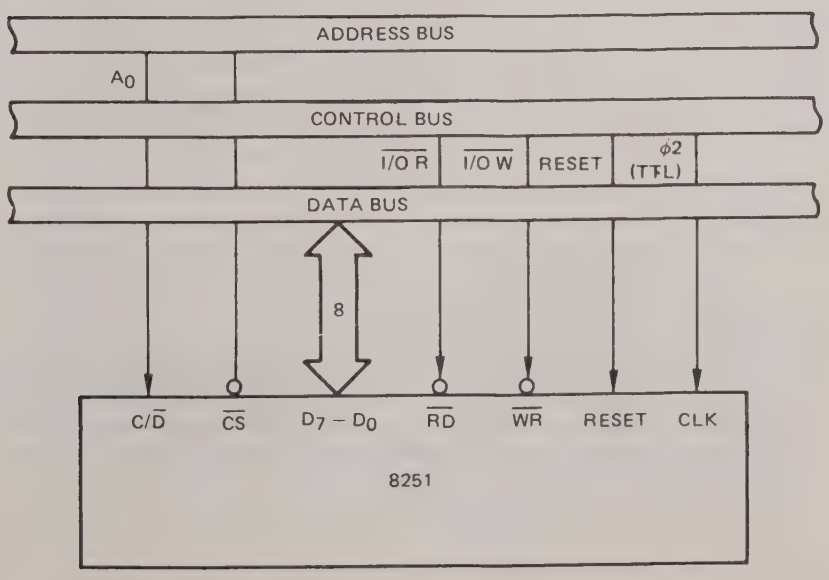
TRANSMIT BUFFER/ CONVERTER

The Transmit Buffer/Converter receives parallel data from the Data Bus Buffer via the internal data bus, converts parallel to serial data, inserts the necessary characters or bits needed for the programmed communication format and outputs composite serial data on the TxD output.

PIN IDENTIFICATION (CONT.)

PIN			FUNCTION
NO.	SYMBOL	NAME	
Transmit Control Logic			The Transmit Control Logic accepts and outputs all external and internal signals necessary for serial data transmission.
15	TxRDY	Transmitter Ready	Transmitter Ready signals the processor that the transmitter is ready to accept a data character. TxRDY can be used as an interrupt or may be tested through the Status information for Polled operation. Loading a character from the processor automatically resets TxRDY.
18	TxE	Transmitter Empty	The Transmitter Empty output signals the processor that the USART has no further characters to transmit. TxE is automatically reset upon receiving a data character from the processor. In half-duplex, TxE can be used to signal end of a transmission and request the processor to "turn the line around." The TxEn bit in the command instruction does not effect TxE. In the Synchronous mode, a "one" on this output indicates that a Sync character or characters are about to be automatically transmitted as "fillers" because the next data character has not been loaded.
9	$\overline{TxC}$	Transmitter Clock	The Transmitter Clock controls the serial character transmission rate. In the Asynchronous mode, the $\overline{TxC}$ frequency is a multiple of the actual Baud Rate. Two bits of the Mode Instruction select the multiple to be 1x, 16x, or 64x the Baud Rate. In the Synchronous mode, the $\overline{TxC}$ frequency is automatically selected to equal the actual Baud Rate. Note that for both Synchronous and Asynchronous modes, serial data is shifted out of the USART by the falling edge of $\overline{TxC}$.
19	TxD	Transmitter Data	The Transmit Control Logic outputs the composite serial data stream on this pin.

8251 INTERFACE TO 8080 STANDARD SYSTEM BUS



RECEIVER BUFFER

The Receiver Buffer accepts serial data input at the $\overline{RxD}$ pin and converts the data from serial to parallel format. Bits or characters required for the specific communication technique in use are checked and then an eight-bit "assembled" character is readied for the processor. For communication techniques which require less than eight bits, the μPD8251 sets the extra bits to "zero."

PIN IDENTIFICATION (CONT.)

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
Receiver Control Logic			This block manages all activities related to incoming data.
14	RxRDY	Receiver Ready	The Receiver Ready output indicates that the Receiver Buffer is ready with an "assembled" character for input to the processor. For Polled operation, the processor can check RxRDY using a Status Read or RxRDY can be connected to the processor interrupt structure. Note that reading the character to the processor automatically resets RxRDY.
25	$\overline{RxC}$	Receiver Clock	The Receiver Clock is the rate at which the incoming character is received. In the Asynchronous mode, the $\overline{RxC}$ frequency may be 1,16 or 64 times the actual Baud Rate but in the Synchronous mode the $\overline{RxC}$ frequency must equal the Baud Rate. Two bits in the mode instruction select Asynchronous at 1x, 16x or 64x or Synchronous operation at 1x the Baud Rate. Unlike $\overline{TxC}$, data is sampled by the μPD8251 on the rising edge of $\overline{RxC}$. (1)
3	RxD	Receiver Data	A composite serial data stream is received by the Receiver Control Logic on this pin.
16	SYNDET	Sync Detect	The SYNC Detect pin is only used in the Synchronous mode. The μPD8251 may be programmed through the Mode Instruction to operate in either the internal or external Sync mode and SYNDET then functions as an output or input respectively. In the internal Sync mode, the SYNDET output will go to a "one" when the μPD8251 has located the SYNC character in the Receive mode. If double SYNC character (bi-sync) operation has been programmed, SYNDET will go to "one" in the middle of the last bit of the second SYNC character. SYNDET is automatically reset to "zero" upon a Status Read or RESET. In the external SYNC mode, a "zero" to "one" transition on the SYNDET input will cause the μPD8251 to start assembling data character on the next falling edge of $\overline{RxC}$. The length of the SYNDET input should be at least one $\overline{RxC}$ period, but may be removed once the μPD8251 is in SYNC.

Note: (1) Since the μPD8251 will frequently be handling both the reception and transmission for a given link, the Receive and Transmit Baud Rates will be same. $\overline{RxC}$ and $\overline{TxC}$ then require the same frequency and may be tied together and connected to a single clock source or Baud Rate Generator.

Examples:

If the Baud Rate equals 110 (Async):	If the Baud Rate equals 300:
$\overline{RxC}$ or $\overline{TxC}$ equals 110 Hz (1x)	$\overline{RxC}$ or $\overline{TxC}$ equals 300 Hz (1x) A or S
$\overline{RxC}$ or $\overline{TxC}$ equals 1.76 KHz (16x)	$\overline{RxC}$ or $\overline{TxC}$ equals 4800 Hz (16x) A only
$\overline{RxC}$ or $\overline{TxC}$ equals 7.04 KHz (64x)	$\overline{RxC}$ or $\overline{TxC}$ equals 19.2 KHz (64x) A only

OPERATIONAL DESCRIPTION

A set of control words must be sent to the μPD8251 to define the desired mode and communications format. The control words will specify the BAUD RATE FACTOR (1x, 16x, 64x), CHARACTER LENGTH (5 to 8), NUMBER OF STOP BITS (1, 1-1/2, 2), ASYNCHRONOUS or SYNCHRONOUS MODE, SYNDET (IN or OUT), PARITY, etc.

After receiving the control words, the μPD8251 is ready to communicate. TxRDY is raised to signal the processor that the USART is ready to receive a character for transmission. When the processor writes a character to the USART, TxRDY is automatically reset.

Concurrently, the μPD8251 may receive serial data; and after receiving an entire character, the RxRDY output is raised to indicate a completed character is ready for the processor. The processor fetch will automatically reset RxRDY.

Note: The μPD8251 may provide faulty RxRDY for the first read after power-on or for the first read after receive is re-enabled by a command instruction (RxE). A dummy read is recommended to clear faulty RxRDY. But this is not the case for the first read after hardware or software reset after the device operation has once been established.

The μPD8251 cannot transmit until the TxEN (Transmitter Enable) bit has been set by a Command Instruction and until the $\overline{CTS}$ (Clear to Send) input is a "zero". TxD is held in the "marking" state after Reset awaiting new Command Words.

μPD8251 PROGRAMMING

The USART must be loaded with a group of two to four control words provided by the processor before data reception and transmission can begin. A Reset (internal or external) must immediately proceed the control words which are used to program the complete operational description of the communications interface. If an external RESET is not available, three successive 00 Hex or two successive 80 Hex command instructions ($C/\overline{D} = 1$) followed by a software reset command instruction (40 Hex) can be used to initialize the 8251.

There are two control word formats:

1. Mode Instruction
2. Command Instruction

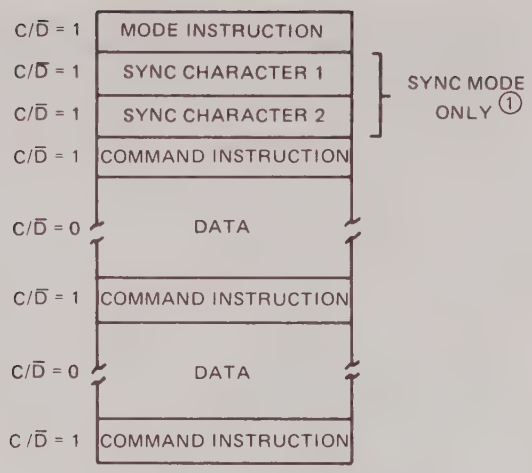
MODE INSTRUCTION

This control word specifies the general characteristics of the interface regarding the SYNCHRONOUS or ASYNCHRONOUS MODE, BAUD RATE FACTOR, CHARACTER LENGTH, PARITY, and NUMBER OF STOP BITS. Once the Mode Instruction has been received, SYNC characters or Command Instructions may be inserted depending on the Mode Instruction content.

COMMAND INSTRUCTION

This control word will be interpreted as a SYNC character definition if immediately preceded by a Mode Instruction which specified a Synchronous format. After the SYNC character(s) are specified or after an Asynchronous Mode Instruction, all subsequent control words will be interpreted as an update to the Command Instruction. Command Instruction updates may occur at any time during the data block. To modify the Mode Instruction, a bit may be set in the Command Instruction which causes an internal Reset which allows a new Mode Instruction to be accepted.

TYPICAL DATA BLOCK



NOTE (1) The second SYNC character is skipped if MODE instruction has programmed the 8251 to single character Internal SYNC Mode. Both SYNC characters are skipped if MODE instruction has programmed the 8251 to ASYNC mode.

MODE INSTRUCTION DEFINITION

The μPD8251 can operate in either Asynchronous or Synchronous communication modes. Understanding how the Mode Instruction controls the functional operation of the USART is easiest when the device is considered to be two separate components, one asynchronous and the other synchronous, which share the same support circuits and package. Although the format definition can be changed at will or "on the fly", the two modes will be explained separately for clarity.

ASYNCHRONOUS TRANSMISSION

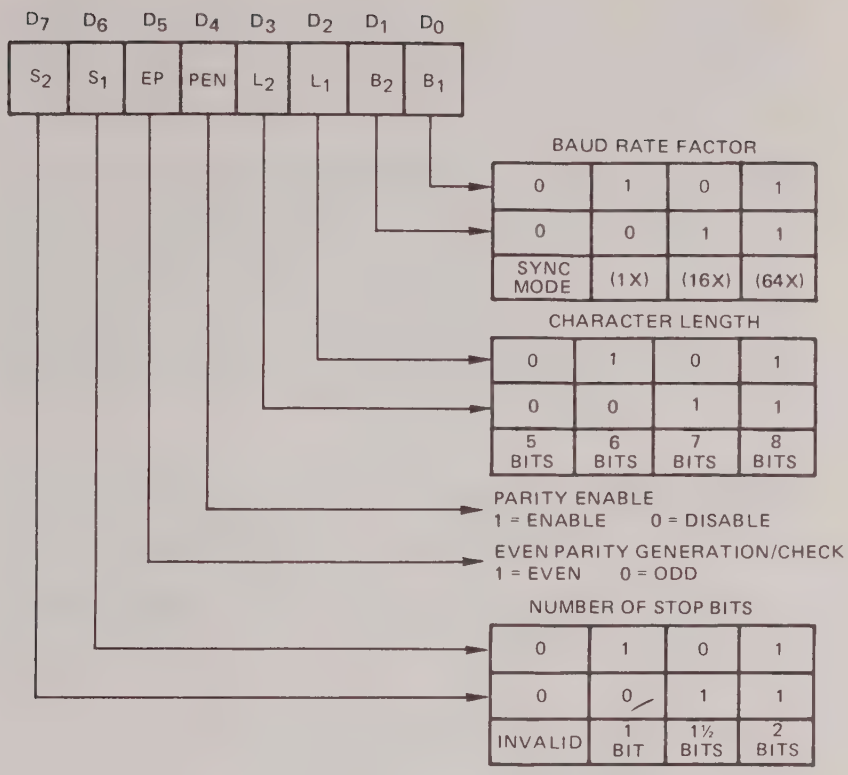
When a data character is written into the μPD8251, the USART automatically adds a START bit (low level or "space") and the number of STOP bits (high level or "mark") specified by the Mode Instruction. If Parity has been enabled, an odd or even Parity bit is inserted just before the STOP bits(s), as specified by the Mode Instruction. Then, depending on $\overline{CTS}$ and TxEN, the character may be transmitted as a serial data stream at the TxD output. Data is shifted out by the falling edge of $\overline{TxC}$ at $\overline{TxC}$, $\overline{TxC}$/16 or $\overline{TxC}$/64, as defined by the Mode Instruction.

If no data characters have been loaded into the μPD8251, or if all available characters have been transmitted, the TxD output remains "high" (marking) in preparation for sending the START bit of the next character provided by the processor. TxD may be forced to send a BREAK (continuously low) by setting the correct bit in the Command Instruction.

ASYNCHRONOUS RECEIVE

The RxD input line is normally held "high" (marking) by the transmitting device. A falling edge at RxD signals the possible beginning of a START bit and a new character. The START bit is checked by testing for a "low" at its nominal center as specified by the BAUD RATE. If a "low" is detected again, it is considered valid, and the bit assembling counter starts counting. The bit counter locates the approximate center of the data, parity (if specified), and STOP bits. The parity error flag (PE) is set, if a parity error occurs. Input bits are sampled at the RxD pin with the rising edge of $\overline{RxC}$. If a high is not detected for the STOP bit, which normally signals the end of an input character, a framing error (FE) will be set. After a valid STOP bit, the input character is loaded into the parallel Data Bus Buffer of the μPD8251 and the RxRDY signal is raised to indicate to the processor that a character is ready to be fetched. If the processor has failed to fetch the previous character, the new character replaces the old and the overrun flag (OE) is set. All the error flags can be reset by setting a bit in the Command Instruction. Error flag conditions will not stop subsequent USART operation.

MODE INSTRUCTION FORMAT ASYNCHRONOUS MODE

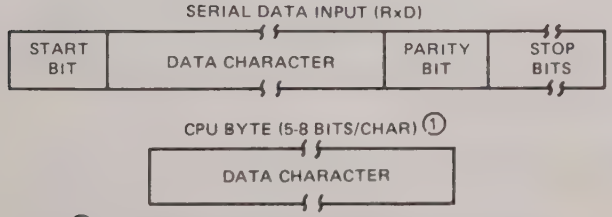

D7 D6 D5 D4 D3 D2 D1 D0
S2 S1 EP PEN L2 L1 B2 B1
BAUD RATE FACTOR
0 1 0 1
0 0 1 1
SYNC MODE (1X) (16X) (64X)
CHARACTER LENGTH
0 1 0 1
0 0 1 1
5 BITS 6 BITS 7 BITS 8 BITS
PARITY ENABLE
1 = ENABLE 0 = DISABLE
EVEN PARITY GENERATION/CHECK
1 = EVEN 0 = ODD
NUMBER OF STOP BITS
0 1 0 1
0 0 1 1
INVALID 1 BIT 1½ BITS 2 BITS

TRANSMIT/RECEIVE FORMAT ASYNCHRONOUS MODE

TRANSMITTER OUTPUT

RECEIVER INPUT

TRANSMISSION FORMAT



NOTE ①: IF CHARACTER LENGTH IS DEFINED AS 5, 6, OR 7 BITS; THE UNUSED BITS ARE SET TO "ZERO."

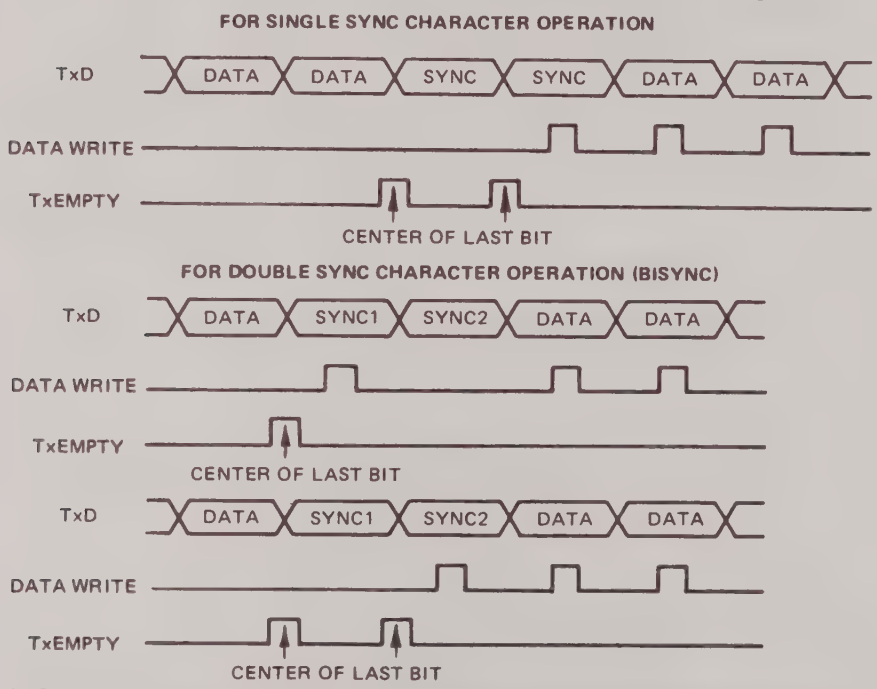
RECEIVE FORMAT

SYNCHRONOUS TRANSMISSION

As in Asynchronous transmission, the TxD output remains "high" (marking) until the μPD8251 receives the first character from the processor which is usually a SYNC character. After a Command Instruction has set TxEN and after Clear to Send ($\overline{CTS}$) goes low, the first character is serially transmitted. Data is shifted out on the falling edge of $\overline{TxC}$ and the same rate as $\overline{TxC}$.

Once transmission has started, Synchronous Mode format requires that the serial data stream at TxD continue at the $\overline{TxC}$ rate or SYNC will be lost. If a data character is not provided by the processor before the μPD8251 Transmitter Buffer becomes empty, the SYNC character(s) loaded directly following the Mode Instruction will be automatically inserted in the TxD data stream. The SYNC character(s) are inserted to fill the line and maintain synchronization until new data characters are available for transmission. If the μPD8251 becomes empty, and must send the SYNC character(s), the TxEMPTY output is raised to signal the processor that the Transmitter Buffer is empty and SYNC characters are being transmitted. TxEMPTY is automatically reset by the next character from the processor.

TxEMPTY go high at the middle of the last data bit when the Transmit Register is EMPTY. TxEMPTY goes low again as sync characters are transmitted. See figure below.



SYNCHRONOUS RECEIVE

In Synchronous Receive, character synchronization can be either external or internal. If the internal SYNC mode has been selected, and the Enter HUNT (EH) bit has been set by a Command Instruction, the receiver goes into the HUNT mode.

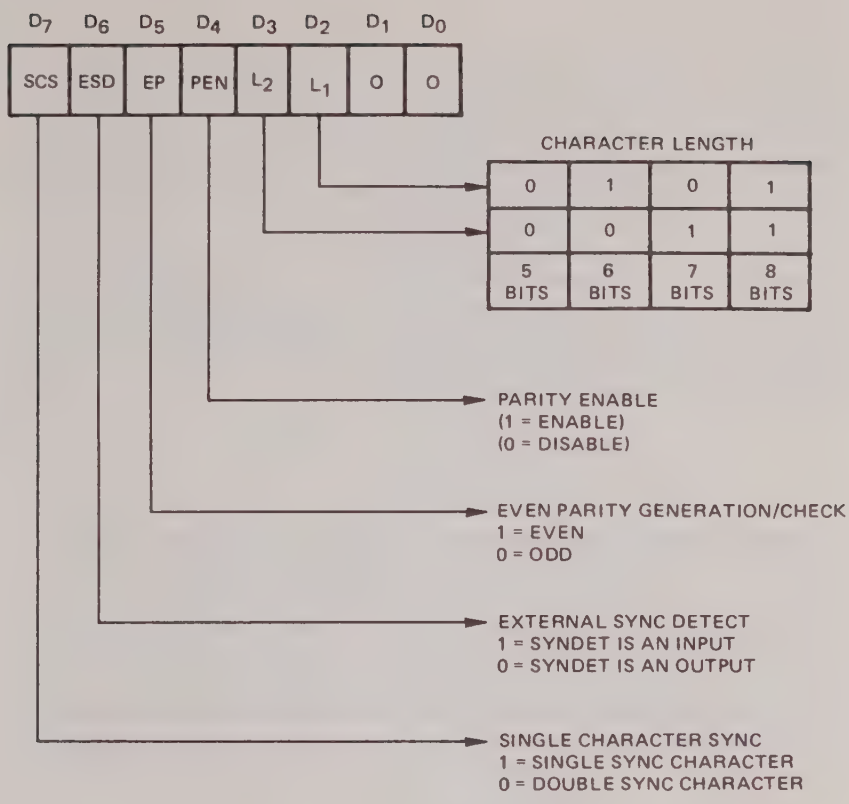
Incoming data on the RxD input is sampled on the rising edge of $\overline{RxC}$, and the Receiver Buffer is compared with the first SYNC character after each bit has been loaded until a match is found. If two SYNC characters have been programmed, the next received character is also compared. When the SYNC character(s) programmed have been detected, the μPD8251 leaves the HUNT mode and is in character synchronization. At this time, the SYNDET (output) is set high. SYNDET is automatically reset by a STATUS READ.

If external SYNC has been specified in the Mode Instruction, a "one" applied to the SYNDET (input) for at least one $\overline{RxC}$ cycle will synchronize the USART.

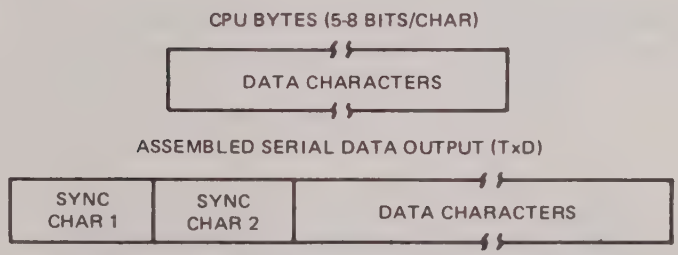
Parity and Overrun Errors are treated the same in the Synchronous as in the Asynchronous Mode. Framing errors do not apply in the Synchronous format.

The processor may command the receiver to enter the HUNT mode with a Command Instruction which sets Enter HUNT (EH) if synchronization is lost.

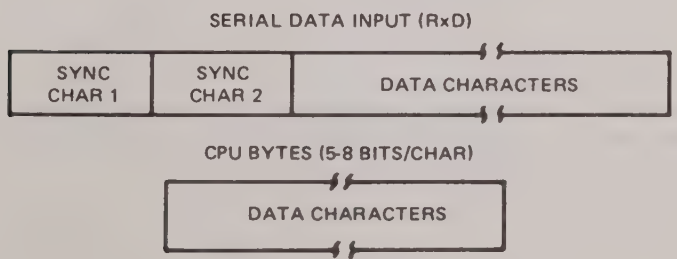
MODE INSTRUCTION FORMAT SYNCHRONOUS MODE


D7 D6 D5 D4 D3 D2 D1 D0
SCS ESD EP PEN L2 L1 0 0
CHARACTER LENGTH
0 1 0 1
0 0 1 1
5 BITS 6 BITS 7 BITS 8 BITS
PARITY ENABLE
(1 = ENABLE)
(0 = DISABLE)
EVEN PARITY GENERATION/CHECK
1 = EVEN
0 = ODD
EXTERNAL SYNC DETECT
1 = SYNDET IS AN INPUT
0 = SYNDET IS AN OUTPUT
SINGLE CHARACTER SYNC
1 = SINGLE SYNC CHARACTER
0 = DOUBLE SYNC CHARACTER

TRANSMIT/RECEIVE FORMAT SYNCHRONOUS MODE



TRANSMIT FORMAT



RECEIVE FORMAT

COMMAND INSTRUCTION FORMAT

After the functional definition of the μPD8251 has been specified by the Mode Instruction and the SYNC character(s) have been entered, if in SYNC mode, the USART is ready to receive Command Instructions and begin communication. A Command Instruction is used to control the specific operation of the format selected by the Mode Instruction. Enable Transmit, Enable Receive, Error Reset and Modem Controls are controlled by the Command Instruction.

After the Mode Instruction and the SYNC character(s), as needed, are loaded, all subsequent "control writes" ($C/\overline{D} = 1$) will load or overwrite the Command Instruction register. A Reset operation (internal via CMD IR or external via the RESET input) will cause the μPD8251 to interpret the next "control write", which must immediately follow the reset, as a Mode Instruction.

STATUS READ FORMAT

It is frequently necessary for the processor to examine the "status" of an active interface device to determine if errors have occurred or to notice other conditions which require a response from the processor. The μPD8251 has features which allow the processor to "read" the device status at any time. A data fetch is issued by the processor while holding the $C/\overline{D}$ input "high" to obtain device Status Information. Many of the bits in the status register are copies of external pins. This dual status arrangement allows the μPD8251 to be used in both Polled and interrupt driven environments. Status update can have a maximum delay of a 16 clock period.

PARITY ERROR

When a parity error is detected, the PE flag is set, and is cleared by setting the ER bit in a subsequent Command Instruction. PE being set does not inhibit USART operation.

OVERRUN ERROR

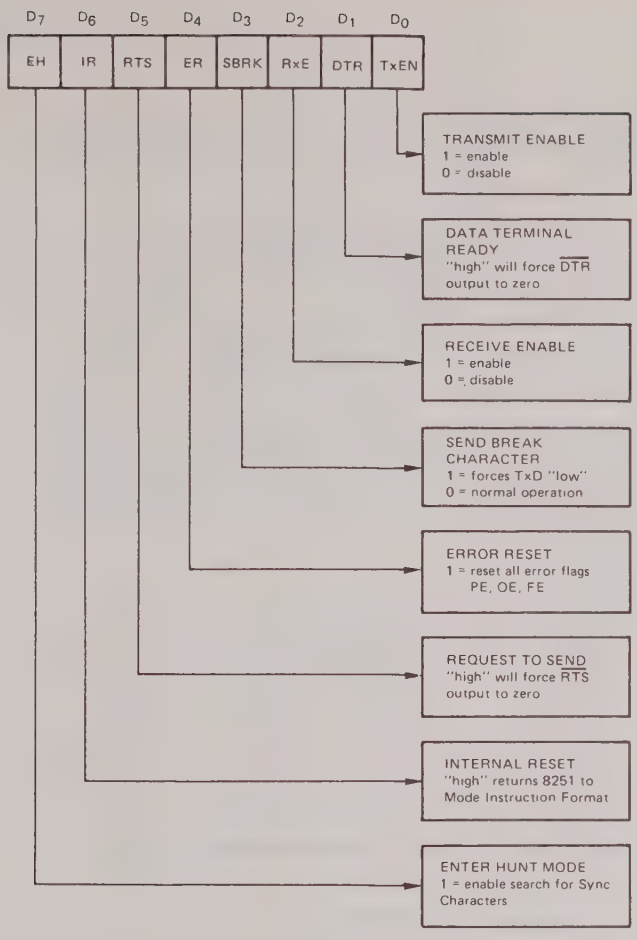
If the processor fails to read a data character before the one following is available, the OE flag is set, and is cleared by setting the ER bit in a subsequent Command Instruction. Although OE being set does not inhibit USART operation, the previously received character is overwritten and lost.

FRAMING ERROR ①

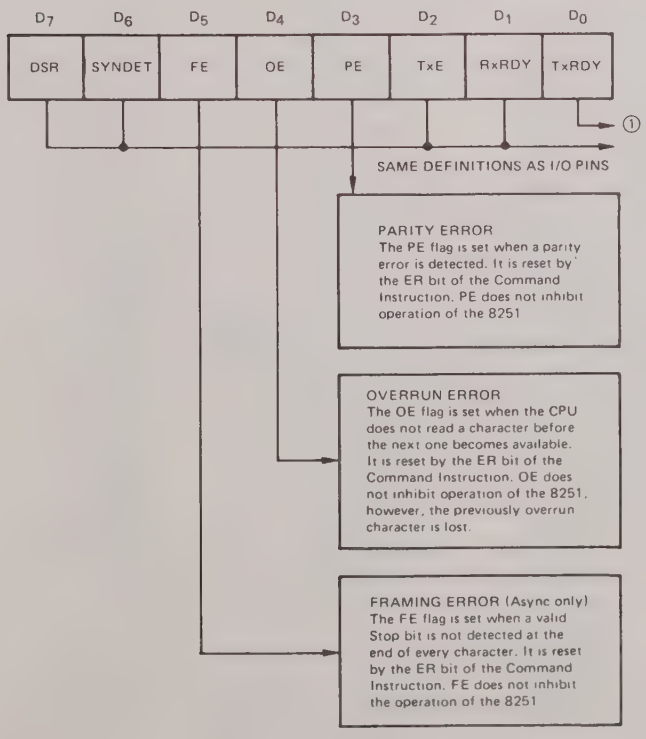
If a valid STOP bit is not detected at the end of a character, the FE flag is set, and is cleared by setting the ER bit in a subsequent Command Instruction. FE being set does not inhibit USART operation.

Note: ① ASYNC mode only.

COMMAND INSTRUCTION FORMAT


D7 D6 D5 D4 D3 D2 D1 D0
EH IR RTS ER SBRK RxE DTR TxEN
TRANSMIT ENABLE
1 = enable
0 = disable
DATA TERMINAL READY
"high" will force DTR output to zero
RECEIVE ENABLE
1 = enable
0 = disable
SEND BREAK CHARACTER
1 = forces TxD "low"
0 = normal operation
ERROR RESET
1 = reset all error flags PE, OE, FE
REQUEST TO SEND
"high" will force RTS output to zero
INTERNAL RESET
"high" returns 8251 to Mode Instruction Format
ENTER HUNT MODE
1 = enable search for Sync Characters

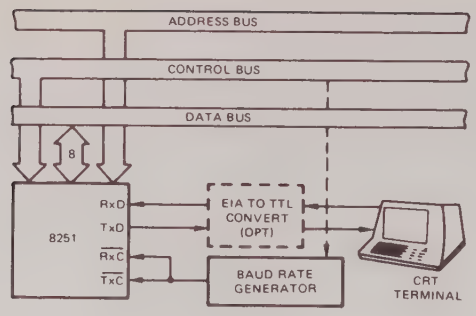
STATUS READ FORMAT


D7 D6 D5 D4 D3 D2 D1 D0
DSR SYNDET FE OE PE TxE RxRDY TxRDY
①
SAME DEFINITIONS AS I/O PINS
PARITY ERROR
The PE flag is set when a parity error is detected. It is reset by the ER bit of the Command Instruction. PE does not inhibit operation of the 8251
OVERRUN ERROR
The OE flag is set when the CPU does not read a character before the next one becomes available. It is reset by the ER bit of the Command Instruction. OE does not inhibit operation of the 8251, however, the previously overrun character is lost.
FRAMING ERROR (Async only)
The FE flag is set when a valid Stop bit is not detected at the end of every character. It is reset by the ER bit of the Command Instruction. FE does not inhibit the operation of the 8251

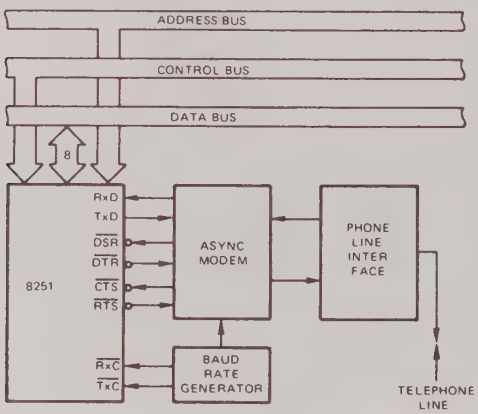
Note: ① TxRDY status bit is not totally equivalent to the TxRDY output pin, the relationship is as follows:

TxRDY status bit = DB Buffer Empty

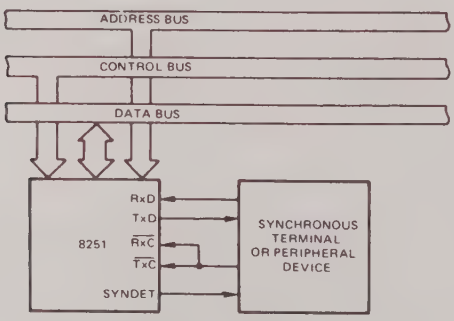
TxRDY (pin 15) = DB Buffer Empty • CTS • TxEn



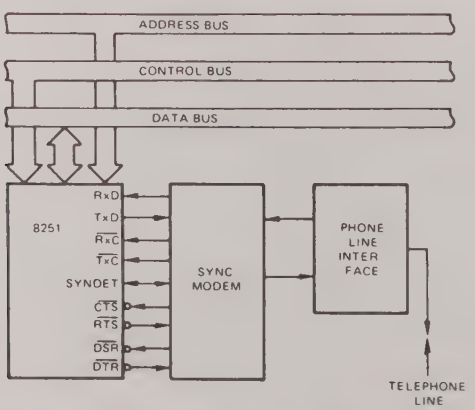
ASYNCHRONOUS SERIAL INTERFACE TO CRT TERMINAL, DC to 9600 BAUD



ASYNCHRONOUS INTERFACE TO TELEPHONE LINES



SYNCHRONOUS INTERFACE TO TERMINAL OR PERIPHERAL DEVICE



SYNCHRONOUS INTERFACE TO TELEPHONE LINES

The information presented in this document is believed to be accurate and reliable. The information is subject to change without notice.

PROGRAMMABLE PERIPHERAL INTERFACES

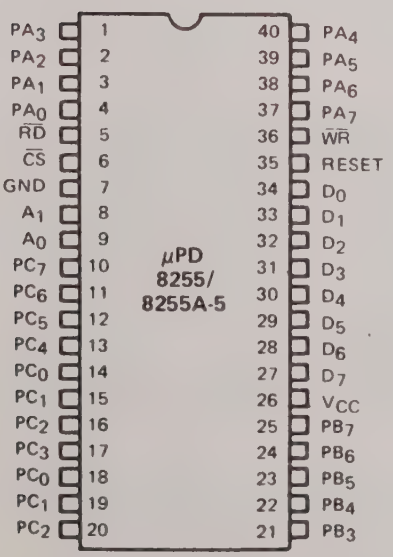
DESCRIPTION

The μPD8255 and μPD8255A-5 are general purpose programmable INPUT/OUTPUT devices designed for use with the 8080A/8085A microprocessors. Twenty-four (24) I/O lines may be programmed in two groups of twelve (group I and group II) and used in three modes of operation. In the Basic mode, (MODE 0), each group of twelve I/O pins may be programmed in sets of 4 to be input or output. In the Strobed mode, (MODE 1), each group may be programmed to have 8 lines of input or output. Three of the remaining four pins in each group are used for handshaking strobes and interrupt control signals. The Bidirectional Bus mode, (MODE 2), uses the 8 lines of Port A for a bidirectional bus, and five lines from Port C for bus control signals. The μPD8255 and μPD8255A-5 are packaged in 40 pin plastic dual-in-line packages.

FEATURES

- Fully Compatible with the 8080A/8085 Microprocessor Families
- All Inputs and Outputs TTL Compatible
- 24 Programmable I/O Pins
- Direct Bit SET/RESET Eases Control Application Interfaces
- 8 – 2 mA Darlington Drive Outputs for Printers and Displays (μPD8255)
- 8 – 4 mA Darlington Drive Outputs for Printers and Displays (μPD8255A-5)
- LSI Drastically Reduces System Package Count
- Standard 40 Pin Dual-In-Line Plastic Package

PIN CONFIGURATION



PIN NAMES

D_7-D_0	Data Bus (Bi-Directional)
RESET	Reset Input
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A_0, A_1	Port Address
PA_7-PA_0	Port A (Bit)
PB_7-PB_0	Port B (Bit)
PC_7-PC_0	Port C (Bit)
V_{CC}	+5 Volts
GND	0 Volts

*All data pertaining to the μPD8255A-5 is preliminary.

FUNCTIONAL DESCRIPTION

General

The μPD8255 and μPD8255A-5 Programmable Peripheral Interfaces (PPI) are designed for use in 8080A/8085A microprocessor systems. Peripheral equipment can be effectively and efficiently interfaced to the 8080A/8085A data and control busses with the μPD8255 and μPD8255A-5. The μPD8255 and μPD8255A-5 are functionally configured to be programmed by system software to avoid external logic for peripheral interfaces.

Data Bus Buffer

The 3-state, bidirectional, eight bit Data Bus Buffer (D_0-D_7) of the μPD8255 and μPD8255A-5 can be directly interfaced to the processor's system Data Bus (D_0-D_7). The Data Bus Buffer is controlled by execution of IN and OUT instructions by the processor. Control Words and Status information are also transmitted via the Data Bus Buffer.

Read/Write and Control Logic

This block manages all of the internal and external transfers of Data, Control and Status. Through this block, the processor Address and Control busses can control the peripheral interfaces.

Chip Select, $\overline{CS}$, pin 6

A Logic Low, V_{IL}, on this input enables the μPD8255 and μPD8255A-5 for communication with the 8080A/8085A.

Read, $\overline{RD}$, pin 5

A Logic Low, V_{IL}, on this input enables the μPD8255 and μPD8255A-5 to send Data or Status to the processor via the Data Bus Buffer.

Write, $\overline{WR}$, pin 36

A Logic Low, V_{IL}, on this input enables the Data Bus Buffer to receive Data or Control Words from the processor.

Port Select 0, A_0, pin 9
Port Select 1, A_1, pin 8

These two inputs are used in conjunction with $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ to control the selection of one of three ports on the Control Word Register. A_0 and A_1 are usually connected to A_0 and A_1 of the processor Address Bus.

Reset, pin 35

A Logic High, V_{IH}, on this input clears the Control Register and sets ports A, B, and C to the input mode. The input latches in ports A, B, and C are not cleared.

Group I and Group II Controls

Through an OUT instruction in System Software from the processor, a control word is transmitted to the μPD8255 and μPD8255A-5. Information such as "MODE," "Bit SET," and "Bit RESET" is used to initialize the functional configuration of each I/O port.

Each group (I and II) accepts "commands" from the Read/Write Control Logic and "control words" from the internal data bus and in turn controls its associated I/O ports.

Group I — Port A and upper Port C (PC_7-PC_4)
Group II — Port B and lower Port C (PC_3-PC_0)

While the Control Word Register can be written into, the contents cannot be read back to the processor.

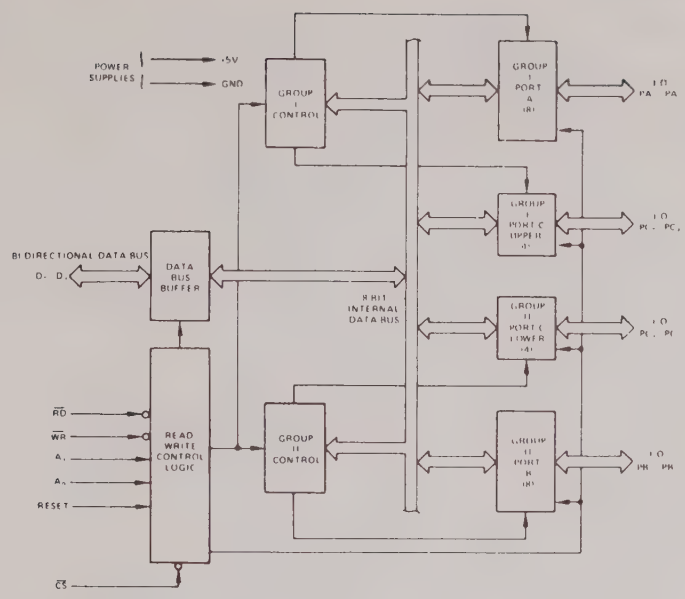
Ports A, B, and C

The three 8-bit I/O ports (A, B, and C) in the μPD8255 and μPD8255A-5 can all be configured to meet a wide variety of functional requirements through system software. The effectiveness and flexibility of the μPD8255 and μPD8255A-5 is further enhanced by special features unique to each of the ports.

Port A = An 8-bit data output latch/buffer and data input latch.
Port B = An 8-bit data input/output latch/buffer and an 8-bit data input buffer.
Port C = An 8-bit output latch/buffer and a data input buffer (input not latched).

Port C may be divided into two independent 4-bit control and status ports for use with Ports A and B.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +125°C
All Output Voltages ①	-0.5 to +7 Volts
All Input Voltages ①	-0.5 to +7 Volts
Supply Voltages ①	-0.5 to +7 Volts

Note: ① With respect to V_{SS}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C, V_{CC} = +5V ± 5%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS μPD8255 MIN	μPD8255 TYP	μPD8255 MAX	LIMITS μPD8255A-5 MIN	μPD8255A-5 TYP	μPD8255A-5 MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	V_{SS}-0.5		0.8	-0.5		0.8	V	
Input High Voltage	V_{IH}	2		V_{CC}	2		V_{CC}	V	
Output Low Voltage	V_{OL}			0.4			0.45	V	②
Output High Voltage	V_{OH}	2.4			2.4			V	③
Darlington Drive Current	I_{OH} ①	-1	-2	-4	-1	-2	-4	mA	V_{OH} = 1.5V, R_{EXT} = 750Ω
Power Supply Current	I_{CC}		40	120		40	120	mA	V_{CC} = +5V, Output Open
Input Leakage Current	I_{LIH}			10			10	μA	V_{IN} = V_{CC}
Input Leakage Current	I_{LIL}			-10			-10	μA	V_{IN} = 0.4V
Output Leakage Current	I_{LOH}			10			10	μA	V_{OUT} = V_{CC}, $\overline{CS}$ = 2.0V
Output Leakage Current	I_{LOL}			10			-10	μA	V_{OUT} = 0.4V, $\overline{CS}$ = 2.0V

Notes ① Any set of eight (8) outputs from either Port A, B, or C can source 2 mA into 1.5V for μPD8255, or 4 mA into 1.5V for μPD8255A-5
② For μPD8255 I_{OL} = 1.7 mA
For μPD8255A-5 I_{OL} = 2.5 mA for DB Port, 1.7 mA for Peripheral Ports
③ For μPD8255 I_{OH} = -100 μs for DB Port, -50 μs for Peripheral Ports
For μPD8255A-5 I_{OH} = -400 μs for DB Port, -200 μs for Peripheral Ports

CAPACITANCE

T_a = 25°C; V_{CC} = V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	f_c = 1 MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to V_{SS}

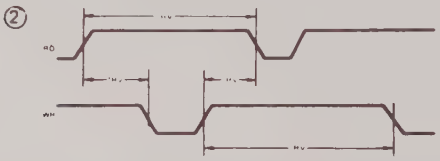
μPD8255/8255A-5

AC CHARACTERISTICS

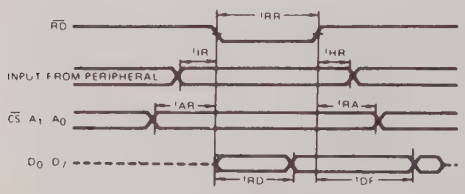
T_a = 0°C to +70°C, V_{CC} = +5V ± 5%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS μPD8255 MIN	LIMITS μPD8255 MAX	LIMITS μPD8255A-5 MIN	LIMITS μPD8255A-5 MAX	UNIT	TEST CONDITIONS
READ							
Address Stable Before $\overline{READ}$	t_{AR}	50		0		ns	
Address Stable After $\overline{READ}$	t_{RA}	0		0		ns	
$\overline{READ}$ Pulse Width	t_{RR}	405		300		ns	
Data Valid From $\overline{READ}$	t_{RD}		295		200	ns	8255, C_L = 100 pF 8255A-5 C_L = 150 pF
Data Float After $\overline{READ}$	t_{DF}	10	150	10	100	ns ns	C_L = 100 pF C_L = 15 pF
Time Between $\overline{READ}$s and/or $\overline{WRITE}$s	t_{RV}	850		850		ns	②
WRITE							
Address Stable Before $\overline{WRITE}$	t_{AW}	20		0		ns	
Address Stable After $\overline{WRITE}$	t_{WA}	20		20		ns	
$\overline{WRITE}$ Pulse Width	t_{WW}	400		300		ns	
Data Valid To $\overline{WRITE}$ (L.E.)	t_{DW}	10		100		ns	
Data Valid After $\overline{WRITE}$	t_{WD}	35		30		ns	
OTHER TIMING							
$\overline{WR}$ = 0 To Output	t_{WB}		500		350	ns	8255 C_L = 50 pF 8255A-5 C_L = 150 pF
Peripheral Data Before $\overline{RD}$	t_{IR}	0		0		ns	
Peripheral Data After $\overline{RD}$	t_{HR}	50		0		ns	
$\overline{ACK}$ Pulse Width	t_{AK}	500		300		ns	
$\overline{STB}$ Pulse Width	t_{ST}	350		500		ns	
Per. Data Before T.E. Of $\overline{STB}$	t_{PS}	60		0		ns	
Per. Data After T.E. Of $\overline{STB}$	t_{PH}	150		180		ns	
$\overline{ACK}$ = 0 To Output	t_{AD}		400		300	ns	8255 C_L = 50 pF 8255A-5 C_L = 150 pF
$\overline{ACK}$ = 0 To Output Float	t_{KD}	20	300	20	250	ns	8256 C_L = 50 pF 8256 C_L = 15 pF
$\overline{WR}$ = 1 To $\overline{OBF}$ = 0	t_{WOB}		300		650	ns	
$\overline{ACK}$ = 0 To $\overline{OBF}$ = 1	t_{AOB}		450		350	ns	
$\overline{STB}$ = 0 To IBF = 1	t_{SIB}		450		300	ns	
$\overline{RD}$ = 1 To IBF = 0	t_{RIB}		360		300	ns	8255 C_L = 50 pF
$\overline{RD}$ = 0 To INTR = 0	t_{RIT}		450		400	ns	
$\overline{STB}$ = 1 To INTR = 1	t_{SIT}		400		300	ns	8255A-5 C_L = 150 pF
$\overline{ACK}$ = 1 To INTR = 1	t_{AIT}		400		350	ns	
$\overline{WR}$ = 0 To INTR = 0	t_{WIT}		850		850	ns	

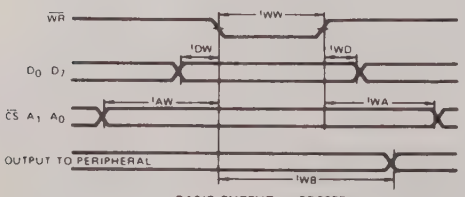
Notes: ① Period of Reset pulse must be at least 50 μs during or after power on. Subsequent Reset pulse can be 500 ns min.

② 

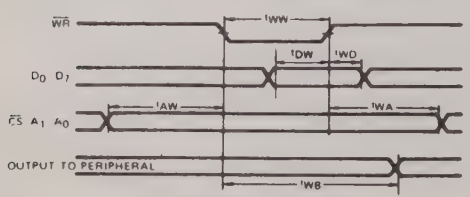
TIMING WAVEFORMS
MODE 0



BASIC INPUT



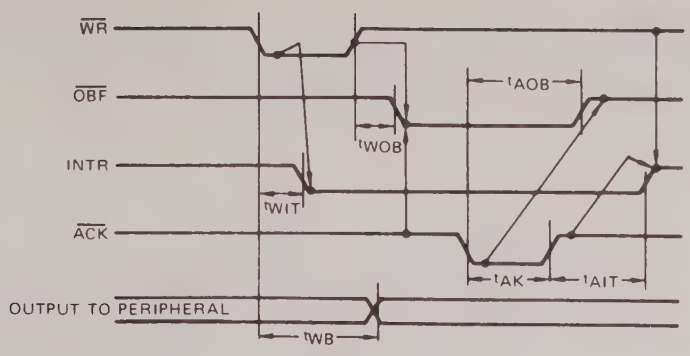
BASIC OUTPUT – μPD8255

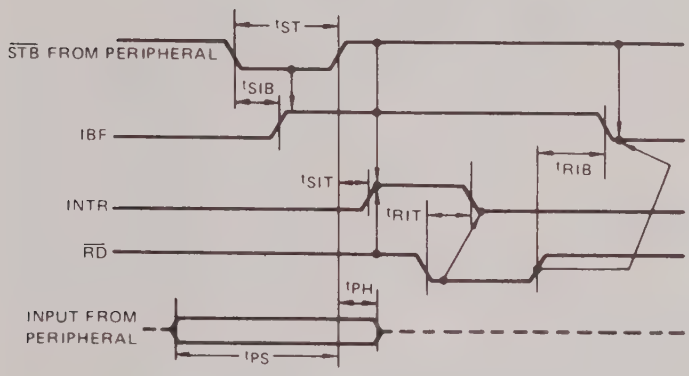


BASIC OUTPUT – μPD8255A-5

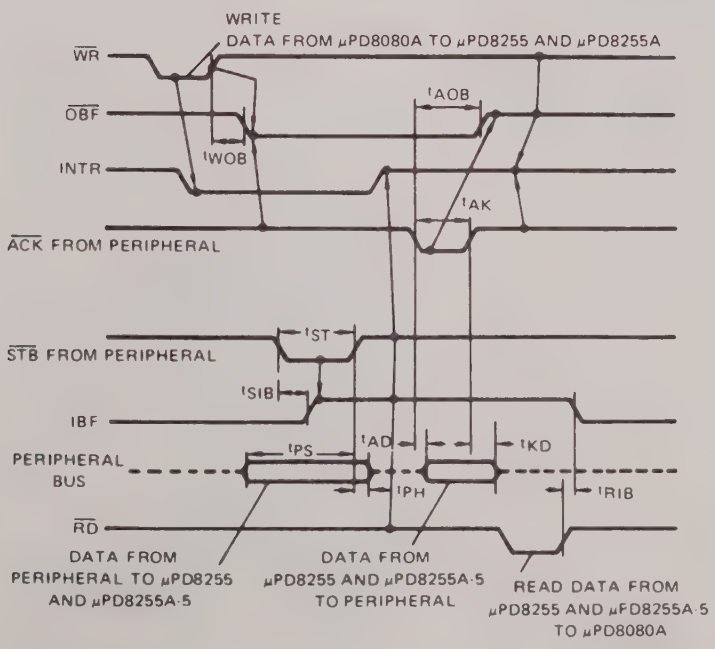
TIMING WAVEFORMS (CONT.)

MODE 1





MODE 2



Note: ① Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
(INTR = IBF · $\overline{MASK}$ · $\overline{STB}$ · $\overline{RD}$ + $\overline{OBF}$ · $\overline{MASK}$ · $\overline{ACK}$ · $\overline{WR}$)

② When the μPD8255A-5 is set to Mode 1 or 2, $\overline{OBF}$ is reset to be high (logic 1).

μPD8255/8255A-5

MODES

The μPD8255 and μPD8255A-5 can be operated in modes (0, 1 or 2) which are selected by appropriate control words and are detailed below.

MODE 0

- MODE 0 provides for basic Input and Output operations through each of the ports A, B, and C. Output data is latched and input data follows the peripheral. No "handshaking" strobes are needed.

  16 different configurations in MODE 0

  Two 8-bit ports and two 4-bit ports

  Inputs are not latched

  Outputs are latched

MODE 1

MODE 1 provides for Strobed Input and Output operations with data transferred through Port A or B and handshaking through Port C.

Two I/O Groups (I and II)

Both groups contain an 8-bit data port and a 4-bit control/data port

Both 8-bit data ports can be either Latched Input or Latched Output

MODE 2

MODE 2 provides for Strobed bidirectional operation using PA_{0-7} as the bidirectional latched data bus. PC_{3-7} is used for interrupts and "handshaking" bus flow controls similar to Mode 1. Note that PB_{0-7} and PC_{0-2} may be defined as Mode 0 or 1, input or output in conjunction with Port A in Mode 2.

An 8-bit latched bidirectional bus port (PA_{0-7}) and a 5-bit control port (PC_{3-7})

Both inputs and outputs are latched

An additional 8-bit input or output port with a 3-bit control port

BASIC OPERATION

INPUT OPERATION (READ)					
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	0	1	0	PORT A → DATA BUS
0	1	0	1	0	PORT B → DATA BUS
1	0	0	1	0	PORT C → DATA BUS

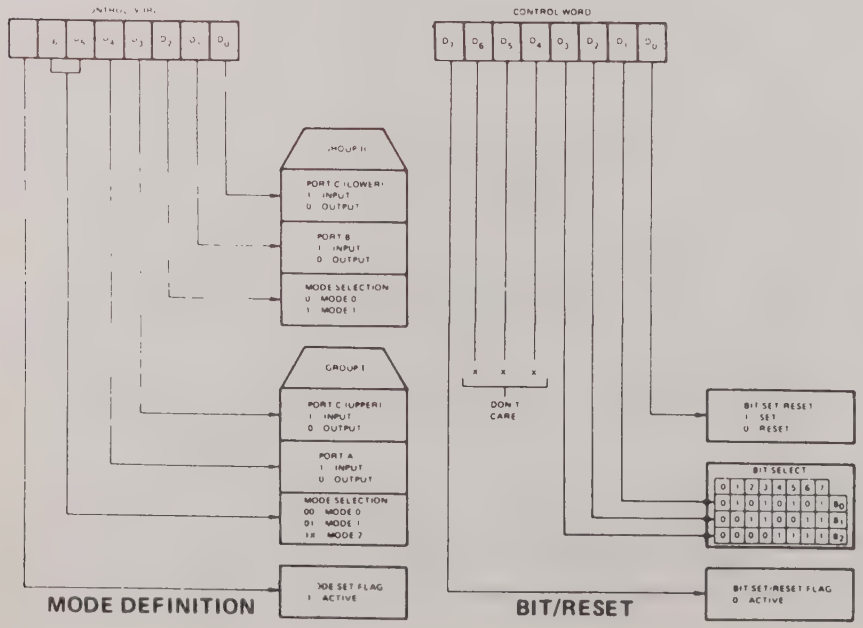
OUTPUT OPERATION (WRITE)					
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	0	DATA BUS → PORT A
0	1	1	0	0	DATA BUS → PORT B
1	0	1	0	0	DATA BUS → PORT C
1	1	1	0	0	DATA BUS → CONTROL

DISABLE FUNCTION					
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
X	X	X	X	1	DATA BUS → HIGH Z STATE
X	X	1	1	0	DATA BUS → HIGH Z STATE

NOTES ① X means "DO NOT CARE"

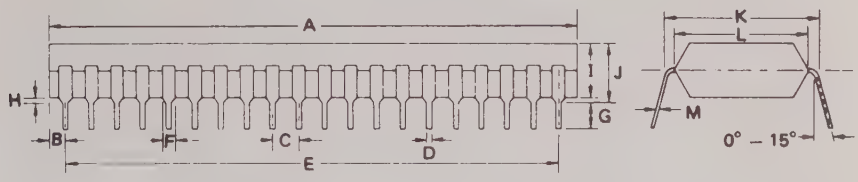
② All conditions not listed are illegal and should be avoided

FORMATS



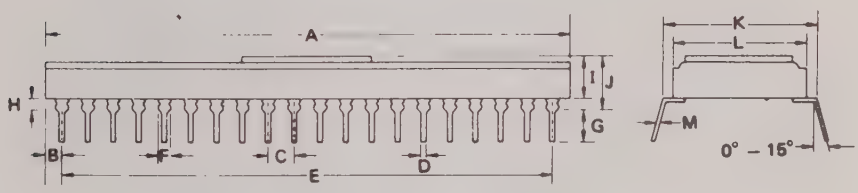
PACKAGE OUTLINE
μPD8255C/D
μPD8255AC/D-5

Members of the μPD8085 Family are housed in both plastic and ceramic 40 pin packages. The drawings and tables below apply to all five of the NEC Microcomputer parts covered in this data sheet.



Plastic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$



Ceramic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.100 ± 0.004
D	0.50 ± 0.1	0.0197 ± 0.004
E	48.26 ± 0.2	1.900 ± 0.008
F	1.27	0.050
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.205 MAX
K	15.24 ± 0.1	0.6 ± 0.004
L	$13.5^{+0.2}_{-0.25}$	$0.531^{+0.008}_{-0.010}$
M	0.30 ± 0.1	0.012 ± 0.004

MULTI-PROTOCOL SERIAL CONTROLLER

DESCRIPTION

The μPD7201 is a dual-channel multi-function peripheral controller designed to satisfy a wide variety of serial data communication requirements in microcomputer systems. Its basic function is a serial-to-parallel, parallel-to-serial converter/controller and within that role it is configurable by systems software so its "personality" can be optimized for a given serial data communications application.

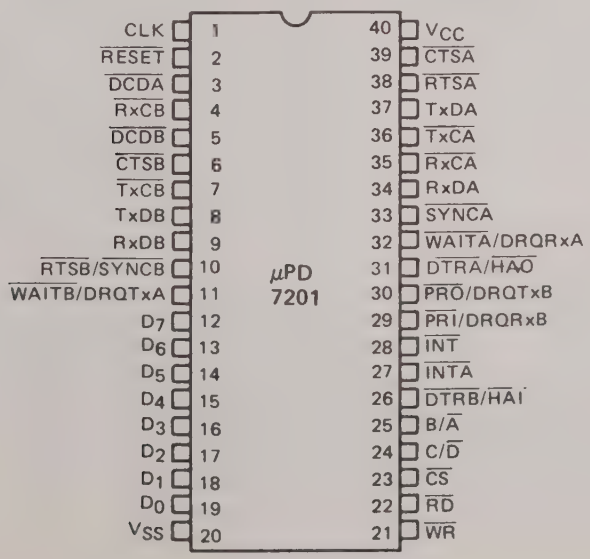
The μPD7201 is capable of handling asynchronous and synchronous byte-oriented protocols such as IBM Bisync, and synchronous bit-oriented protocols such as HDLC and IBM SDLC. This versatile device can also be used to support virtually any other serial protocol for applications other than data communications.

The μPD7201 can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The device also has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

FEATURES

- Two Fully Independent Duplex Serial Channels
- Four Independent DMA Channels for Send/Received Data for Both Serial Inputs/Outputs
- Programmable Interrupt Vectors and Interrupt Priorities
- Modem Controls Signals
- Variable, Software Programmable Data Rate, Up to 880K Baud at 3 MHz Clock
- Double Buffered Transmitter Data and Quadruply Buffered Received Data
- Programmable CRC Algorithm
- Selection of Interrupt, DMA or Polling Mode of Operation
- Asynchronous Operation:
  - Character Length: 5, 6, 7 or 8 Bits
  - Stop Bits: 1, 1-1/2, 2
  - Transmission Speed: x1, x16, x32 or x64 Clock Frequency
  - Parity: Odd, Even, or Disable
  - Break Generation and Detection
  - Interrupt on Parity, Overrun, or Framing Errors
- Monosync, Bisync, and External Sync Operations:
  - Software Selectable Sync Characters
  - Automatic Sync Insertion
  - CRC Generation and Checking
- HDLC and SDLC Operations:
  - Abort Sequence Generation and Detection
  - Automatic Zero Insertion and Detection
  - Address Field Recognition
  - CRC Generation and Checking
  - I-Field Residue Handling
- N-Channel MOS Technology
- Single +5V Power Supply; Interface to Most Microprocessors Including 8080, 8085, 8086 and Others.
- Single Phase TTL Clock
- Available in Plastic and Ceramic Dual-in-Line Packages

PIN CONFIGURATION



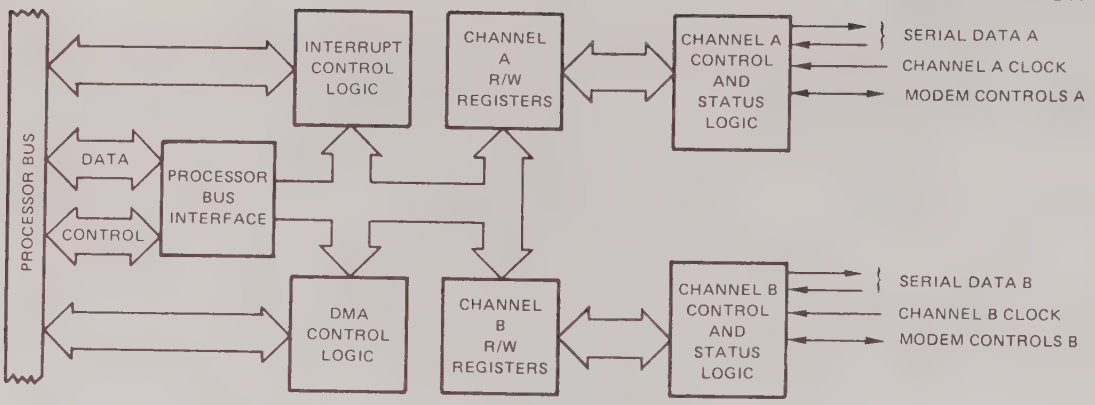
PIN DESCRIPTION

NO.	PIN SYMBOL	PIN NAME	DESCRIPTION
12-19	D_0-D_7	System Data Bus (bidirectional, 3-state)	The system data bus transfers data and commands between the processor and the μPD7201. D_0 is the least significant bit.
25	B/$\overline{A}$	Channel A or B Select (input, High selects Channel B)	This input defines which channel is accessed during a data transfer between the processor and the μPD7201.
24	C/$\overline{D}$	Control or Data Select (input, High selects Control)	This input defines the type of information transfer performed between the processor and the μPD7201. A High at this input during a processor write to or read from the μPD7201 causes the information on the data bus to be interpreted as a command for the channel selected by B/$\overline{A}$. A low at C/$\overline{D}$ means that the information on the data bus is data.
23	$\overline{CS}$	Chip Select (input, active Low)	A low level at this input enables the μPD7201 to accept command or data inputs from the processor during a write cycle, or to transmit data to the processor during a read cycle.
1	CLK	System Clock (input)	The μPD7201 uses standard TTL clock.
22	$\overline{RD}$	Read (input active Low)	If $\overline{RD}$ is active, a memory or I/O read operation is in progress. $\overline{RD}$ is used with C/$\overline{D}$, B/$\overline{A}$ and $\overline{CS}$ to transfer data from the μPD7201 to the processor or the memory.
21	$\overline{WR}$	Write (input, active Low)	The $\overline{WR}$ signal is used to control the transfer of either command or data from the processor or the memory to the μPD7201.
2	$\overline{RESET}$	Reset (input, active Low)	A low $\overline{RESET}$ disables both receivers and transmitters, forces TxDA and TxDB marking, forces the modem controls high and disables all interrupts. The control registers must be rewritten after the μPD7201 is reset and before data is transmitted or received. $\overline{RESET}$ must be active for a minimum of one complete CLK cycle.
10,38	$\overline{RTSA}$, $\overline{RTSB}$	Request to Send (outputs, active Low)	When the $\overline{RTS}$ bit is set, the $\overline{RTS}$ output goes Low. When the $\overline{RTS}$ bit is reset in the Asynchronous mode, the output goes High after the transmitter is empty. In Synchronous modes, the RTS pin strictly follows the state of the $\overline{RTS}$ bit. Both pins can be used as general-purpose outputs.
10,33	$\overline{SYNCA}$, $\overline{SYNCB}$	Synchronization (inputs/outputs, active Low)	These pins can act either as inputs or outputs. In the Asynchronous Receive mode, they are inputs similar to $\overline{CTS}$ and $\overline{DCD}$. In this mode, the transitions on these lines affect the state of the Sync/Hunt status bits in Read Register 0. In the External Sync mode, these lines also act as inputs. When external synchronization is achieved, $\overline{SYNC}$ must be driven Low on the second rising edge of $\overline{RxC}$ after that rising edge of $\overline{RxC}$ on which the last bit of the sync character was received. In other words, after the sync pattern is detected, the external logic must wait for two full Receive Clock cycles to activate the $\overline{SYNC}$ input. Once $\overline{SYNC}$ is forced Low, it is wise to keep it Low until the processor informs the external sync logic that synchronization has been lost or a new message is about to start. Character assembly begins on the rising edge of $\overline{RxC}$ that immediately precedes the falling edge of $\overline{SYNC}$ in the External Sync mode. In the Internal Synchronization mode (Monosync and Bisync), these pins act as outputs that are active during the part of the receive clock ($\overline{RxC}$) cycle in which sync characters are recognized. The sync condition is not latched, so these outputs are active each time a sync pattern is recognized, regardless of character boundaries.
26,31	$\overline{DTRA}$, $\overline{DTRB}$	Data Terminal Ready (outputs, active Low)	These outputs follow the state programmed into the DTR bit. They can also be programmed as general-purpose outputs.

PIN DESCRIPTION (CONT.)

PIN NO.	PIN SYMBOL	PIN NAME	DESCRIPTION
27	$\overline{INTA}$	Interrupt Acknowledge (input, active Low)	This signal is generated by the processor and is sent to all peripheral devices. It serves to acknowledge the interrupt and to allow the highest priority interrupting device to put an 8-bit vector on the bus. $\overline{INT}$ and $\overline{INTA}$ are compatible with the fully nested option of the μPD8259A-5.
29	$\overline{PRI}$	Priority In (input, active Low)	These signals are daisy chained through the peripheral device controllers. The signal on these lines is intact until a device with a pending interrupt request is found on the chain. After that device, this signal holds off lower priority device interrupts. A higher priority device can interrupt the processing of an interrupt from a lower priority device, provided the processor has interrupts enabled. $\overline{PRI}$ is used with $\overline{PRO}$ to form a priority daisy chain when there is more than one interrupt-driven device. A Low on this line indicates that no other device of higher priority is being serviced by a processor interrupt service routine. $\overline{PRO}$ is Low only if $\overline{PRI}$ is Low and the processor is not servicing an interrupt from the μPD7201. Thus, this signal blocks lower priority devices from interrupting while a higher priority device is being serviced by its processor interrupt service routine.
30	$\overline{PRO}$	Priority Out (output, active Low)	
11,29, 30,32	DRQTxA, DRQTxB DRQRxA, DRQRxB	DMA Request (outputs, active High)	These signals are generated by the receiver or transmitter of Channel A and Channel B. These signals can be connected to an 8257 DMA Controller and are used for handshaking during DMA transfer.
26	$\overline{HAI}$	DMA Acknowledge (input, active Low)	Typically, the HLDA signal driven from the processor is input to the $\overline{HAI}$ terminal of the highest priority μPD7201, and the $\overline{HAO}$ output of that μPD7201 is daisy chained to the $\overline{HAI}$ input of the lower priority μPD7201 and propagated downstream. $\overline{HAI}$ and $\overline{HAO}$ signals provide acknowledgement for the highest priority outstanding DMA request.
31	$\overline{HAO}$	DMA Acknowledge (output, active Low)	
28	$\overline{INT}$	Interrupt Request (output, open collector, active Low)	When the μPD7201 is requesting an interrupt, it pulls $\overline{INT}$ low.
11,32	$\overline{WAITA}$, $\overline{WAITB}$	(Outputs, open drain)	Wait lines for both channels that synchronize the processor to the μPD7201 data rate. The reset state is open drain.
6,39	$\overline{CTSA}$, $\overline{CTSB}$	Clear to Send (inputs, active Low)	When programmed as Auto Enables, a Low on these inputs enables the respective transmitter. If not programmed as Auto Enables, these inputs may be programmed as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow-risetime inputs. The μPD7201 detects pulses on these inputs and interrupts the processor on both logic level transitions. The Schmitt-trigger inputs do not guarantee a specified noise-level margin.
3,5	$\overline{DCDA}$, $\overline{DCDB}$	Data Carrier Detect (inputs, active Low)	These signals are similar to the $\overline{CTS}$ inputs, except they can be used as receiver enables.
9,34	RxDA, RxDB	Receive Data (inputs, active High)	
8,37	TxDA, TxDB	Transmit Data (outputs, active High)	
4,35	$\overline{RxCA}$, $\overline{RxCB}$	Receiver Clocks (inputs)	The Receiver Clocks may be 1, 16, 32, or 64 times the data rate in asynchronous modes. Receive data is sampled on the rising edge of $\overline{RxC}$.
7,36	$\overline{TxCA}$, $\overline{TxCB}$	Transmitter Clocks (inputs)	In asynchronous modes, the Transmitter Clocks may be 1, 16, 32, or 64 times the data rate. The multiplier for the transmitter and the receiver must be the same. Both $\overline{TxC}$ and $\overline{RxC}$ inputs are Schmitt-trigger buffered for relaxed rise- and fall-time requirements (no noise margin is specified). TxD changes on the falling edge of $\overline{TxC}$. Note that $\overline{TxC}$ and $\overline{RxC}$ in Channel B are on a common pin, $\overline{RxCB}/\overline{TxCB}$.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Operating Temperature . . . . . 0° to +70°C
Storage Temperature . . . . . −65° to +125°C
Voltage on Any Pin . . . . . −0.5 to +7 Volts ①

Note: ① With respect to ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	−0.5	+0.8	V	
Input High Voltage	V_{IH}	+2.0	V_{CC}+0.5	V	
Output Low Voltage	V_{OL}		+0.45	V	I_{OL} = +2.0 mA
Output High Voltage	V_{OH}	+2.4		V	I_{OH} = −200 μA
Input Leakage Current	I_{IL}		±10	μA	$V_{IN} = V_{CC}$ to 0V
Output Leakage Current	I_{OL}		±10	μA	$V_{OUT} = V_{CC}$ to 0V
V_{CC} Supply Current	I_{CC}		180	mA	

CAPACITANCE

$T_a = 25°C$; $V_{CC} = GND = 0V$

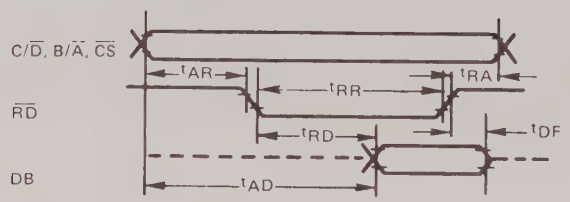
PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		10	pF	fc = 1 MHz
Output Capacitance	C_{OUT}		15	pF	Unmeasured pins Returned to GND
Input/Output Capacitance	$C_{I/O}$		20	pF	

AC CHARACTERISTICS $T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 10\%$

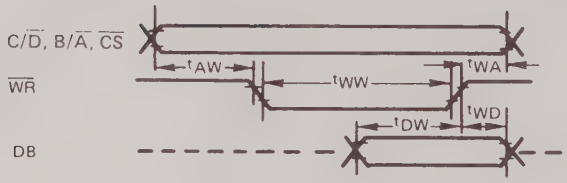
PARAMETER	SYMBOL	LIMITS		UNIT
		MIN	MAX	
Clock Cycle	t_{CY}	250	4000	ns
Clock High Width	t_{CH}	105	2000	ns
Clock Low Width	t_{CL}	105	2000	ns
Clock Rise and Fall Time	t_r, t_f	0	30	ns
Address Setup to $\overline{RD}$	t_{AR}	0		ns
Address Hold from $\overline{RD}$	t_{RA}	0		ns
$\overline{RD}$ Pulse Width	t_{RR}	250		ns
Data Delay from Address	t_{AD}		200	ns
Data Delay from $\overline{RD}$	t_{RD}		200	ns
Output Float Delay	t_{DF}	10	100	ns
Address Setup to $\overline{WR}$	t_{AW}	0		ns
Address Hold from $\overline{WR}$	t_{WA}	0		ns
$\overline{WR}$ Pulse Width	t_{WW}	250		ns
Data Setup to $\overline{WR}$	t_{DW}		150	ns
Data Hold from $\overline{WR}$	t_{WD}	0		ns
$\overline{PRO}$ Delay from $\overline{INTA}$	t_{IAPO}		200	ns
$\overline{PRI}$ Setup to $\overline{INTA}$	t_{PIN}	0		ns
$\overline{PRI}$ Hold from $\overline{INTA}$	t_{IP}	0		ns
$\overline{INTA}$ Pulse Width	t_{II}	250		ns
$\overline{PRO}$ Delay from $\overline{PRI}$	t_{PIPO}		100	ns
Data Delay from $\overline{INTA}$	t_{ID}		200	ns
Request Hold from $\overline{RD}/\overline{WR}$	t_{CO}		150	ns
$\overline{HAI}$ Setup to $\overline{RD}/\overline{WR}$	t_{LR}	300		ns
$\overline{HAI}$ Hold from $\overline{RD}/\overline{WR}$	t_{RL}	0		ns
$\overline{HAO}$ Delay from $\overline{HAI}$	t_{HIHO}		100	ns
Recovery Time Between Controls	t_{RV}	300		ns
$\overline{WAIT}$ Delay from Address	t_{CW}		120	ns
Data Clock Cycle	t_{DCY}	400		ns
Data Clock Low Width	t_{DCL}	180		ns
Data Clock High Width	t_{DCH}	180		ns
Tx Data Delay	t_{TD}		300	ns
Data Set up to $\overline{RxC}$	t_{DS}	0		ns
Data Hold from $\overline{RxC}$	t_{DH}	140		ns
$\overline{INT}$ Delay Time from $\overline{TxC}$	t_{ITD}		4 ~ 6	t_{CY}
$\overline{INT}$ Delay Time from $\overline{RxC}$	t_{IRD}		7 ~ 11	t_{CY}
Low Pulse Width	t_{PL}	200		ns
High Pulse Width	t_{PH}	200		ns
External $\overline{INT}$ from $\overline{CST}$, $\overline{DCD}$, $\overline{SYNC}$	t_{IPD}		500	ns
Delay from $\overline{RxC}$ to $\overline{SYNC}$	t_{DRxC}		100	ns

TIMING WAVEFORMS

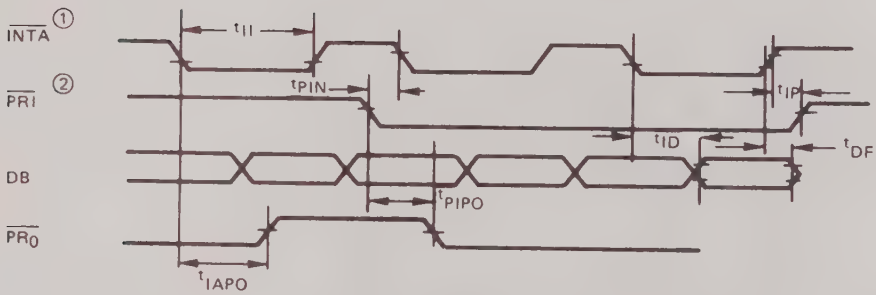
READ CYCLE



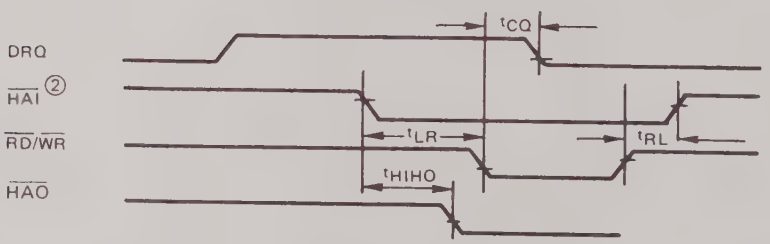
WRITE CYCLE



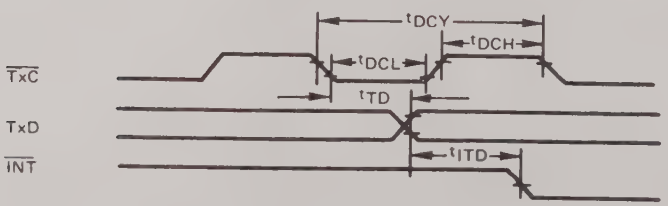
INTA CYCLE



DMA CYCLE



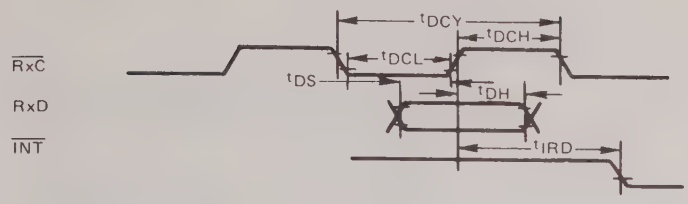
TRANSMIT DATA CYCLE



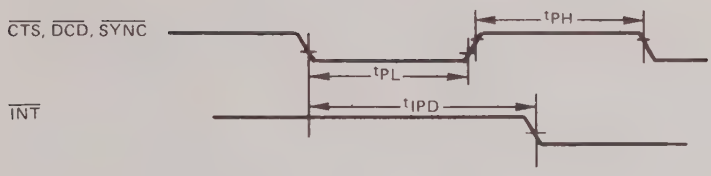
Notes: ① INTA signal acts as RD signal.
② PRI and HAI signals act as CS signal.

TIMING WAVEFORMS (CONT.)

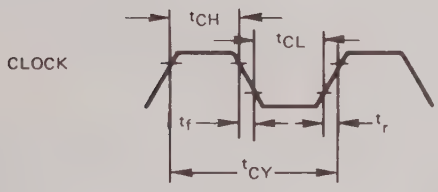
RECEIVE DATA CYCLE



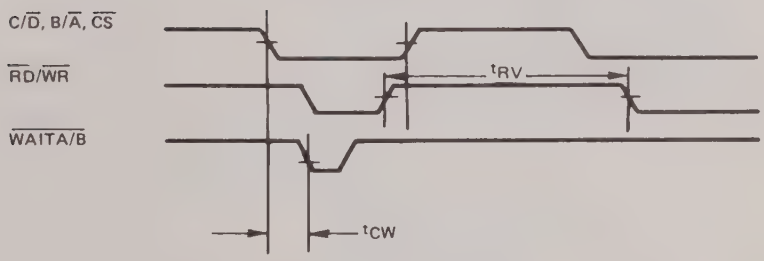
OTHER TIMING



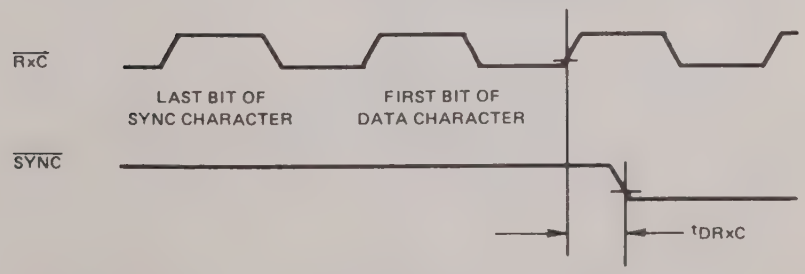
CLOCK



READ/WRITE CYCLE (SOFTWARE BLOCK TRANSFER MODE)

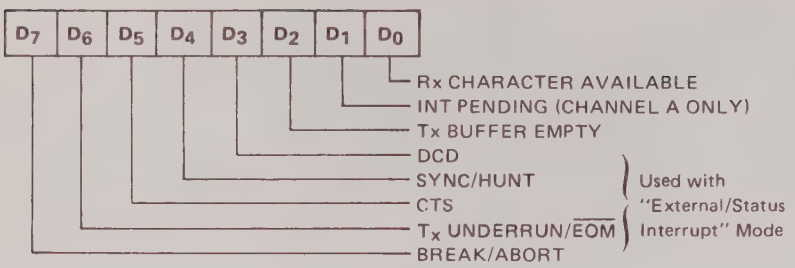


SYNC PULSE GENERATION (EXTERNAL SYNC MODE)

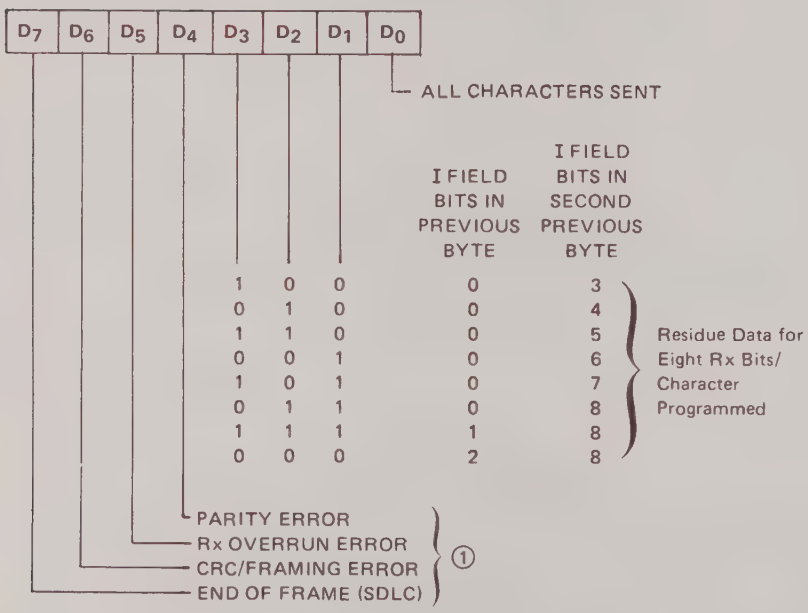


READ REGISTER BIT FUNCTIONS

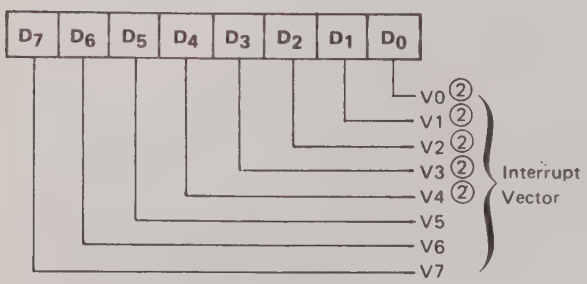
READ REGISTER 0



READ REGISTER 1 ①


D7 D6 D5 D4 D3 D2 D1 D0
ALL CHARACTERS SENT
I FIELD BITS IN PREVIOUS BYTE
I FIELD BITS IN SECOND PREVIOUS BYTE
1 0 0 0 3
0 1 0 0 4
1 1 0 0 5
0 0 1 0 6
1 0 1 0 7
0 1 1 0 8
1 1 1 1 8
0 0 0 2 8
Residue Data for Eight Rx Bits/ Character Programmed
PARITY ERROR
Rx OVERRUN ERROR
CRC/FRAMING ERROR
END OF FRAME (SDLC)
①

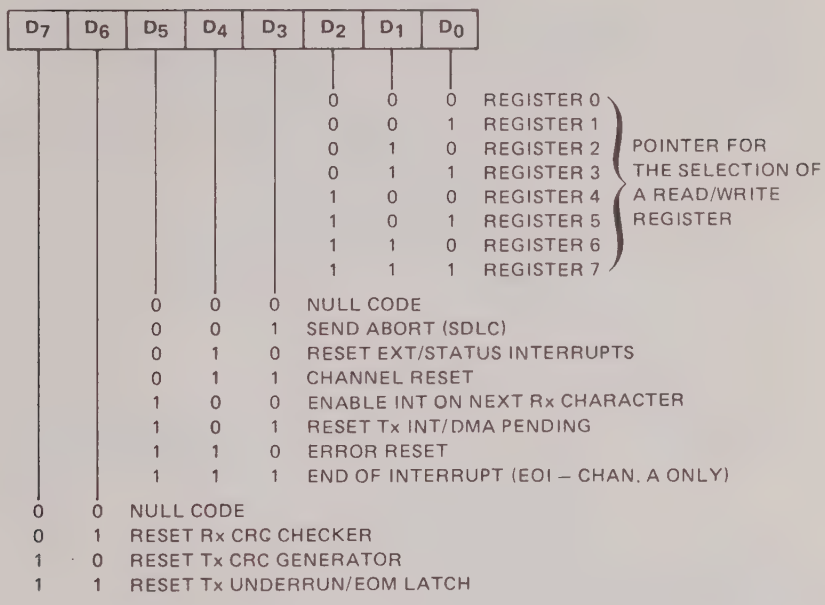
READ REGISTER 2



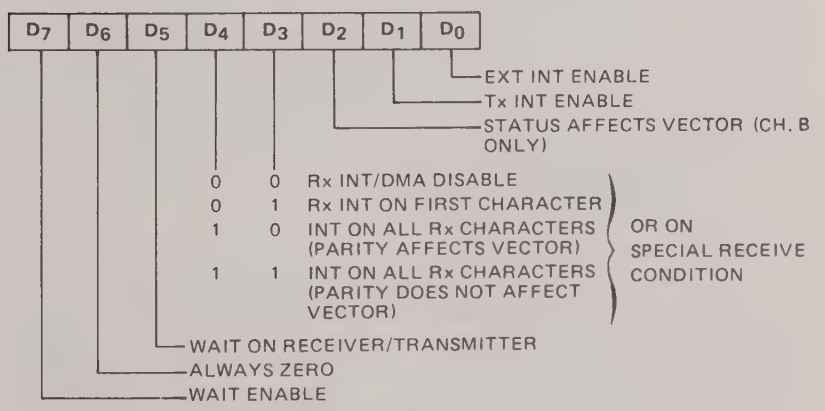
Notes: ① Used with Special Receive Condition Mode.
② Variable if "Status Affects Vector" is programmed.

WRITE REGISTER BIT FUNCTIONS

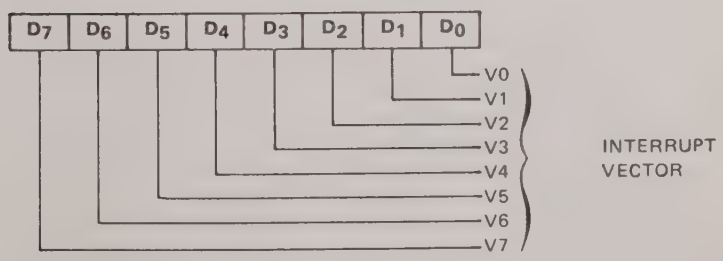
WRITE REGISTER 0


D7 D6 D5 D4 D3 D2 D1 D0
0 0 0 REGISTER 0
0 0 1 REGISTER 1
0 1 0 REGISTER 2
0 1 1 REGISTER 3
1 0 0 REGISTER 4
1 0 1 REGISTER 5
1 1 0 REGISTER 6
1 1 1 REGISTER 7
POINTER FOR THE SELECTION OF A READ/WRITE REGISTER
0 0 0 NULL CODE
0 0 1 SEND ABORT (SDLC)
0 1 0 RESET EXT/STATUS INTERRUPTS
0 1 1 CHANNEL RESET
1 0 0 ENABLE INT ON NEXT Rx CHARACTER
1 0 1 RESET Tx INT/DMA PENDING
1 1 0 ERROR RESET
1 1 1 END OF INTERRUPT (EOI – CHAN. A ONLY)
0 0 NULL CODE
0 1 RESET Rx CRC CHECKER
1 0 RESET Tx CRC GENERATOR
1 1 RESET Tx UNDERRUN/EOM LATCH

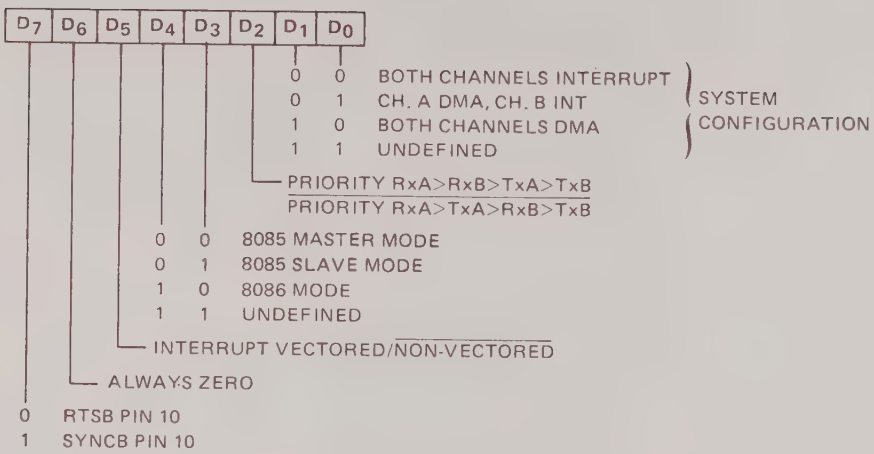
WRITE REGISTER 1


D7 D6 D5 D4 D3 D2 D1 D0
EXT INT ENABLE
Tx INT ENABLE
STATUS AFFECTS VECTOR (CH. B ONLY)
0 0 Rx INT/DMA DISABLE
0 1 Rx INT ON FIRST CHARACTER
1 0 INT ON ALL Rx CHARACTERS (PARITY AFFECTS VECTOR)
1 1 INT ON ALL Rx CHARACTERS (PARITY DOES NOT AFFECT VECTOR)
OR ON SPECIAL RECEIVE CONDITION
WAIT ON RECEIVER/TRANSMITTER
ALWAYS ZERO
WAIT ENABLE

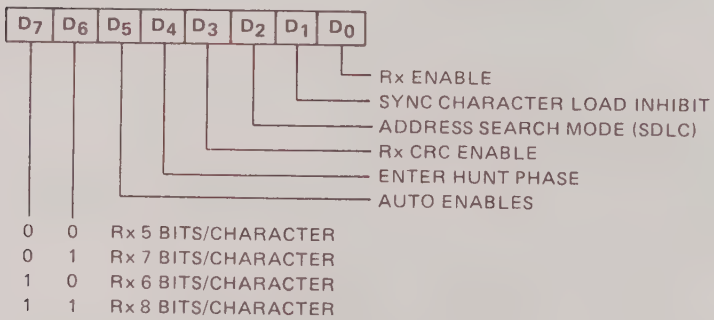
WRITE REGISTER 2 (CHANNEL B)



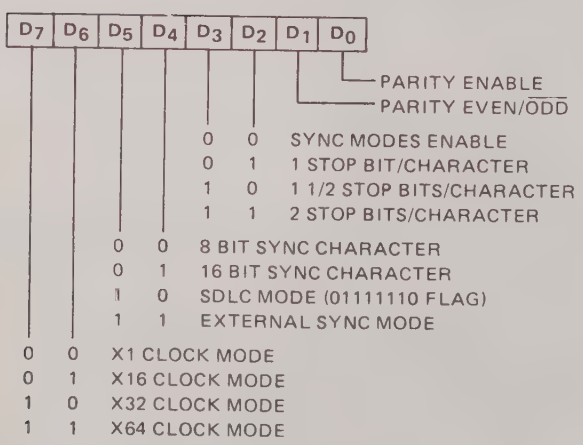
WRITE REGISTER 2 (CHANNEL A)


D7 D6 D5 D4 D3 D2 D1 D0
0 0 BOTH CHANNELS INTERRUPT
0 1 CH. A DMA, CH. B INT
1 0 BOTH CHANNELS DMA
1 1 UNDEFINED
SYSTEM CONFIGURATION
PRIORITY RxA>RxB>TxA>TxB
PRIORITY RxA>TxA>RxB>TxB
0 0 8085 MASTER MODE
0 1 8085 SLAVE MODE
1 0 8086 MODE
1 1 UNDEFINED
INTERRUPT VECTORED/NON-VECTORED
ALWAYS ZERO
0 RTSB PIN 10
1 SYNCB PIN 10

WRITE REGISTER 3

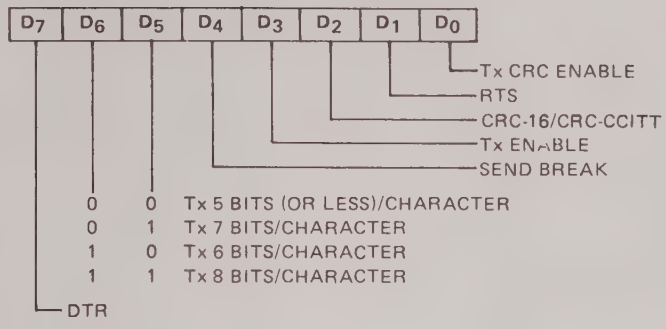

D7 D6 D5 D4 D3 D2 D1 D0
Rx ENABLE
SYNC CHARACTER LOAD INHIBIT
ADDRESS SEARCH MODE (SDLC)
Rx CRC ENABLE
ENTER HUNT PHASE
AUTO ENABLES
0 0 Rx 5 BITS/CHARACTER
0 1 Rx 7 BITS/CHARACTER
1 0 Rx 6 BITS/CHARACTER
1 1 Rx 8 BITS/CHARACTER

WRITE REGISTER 4

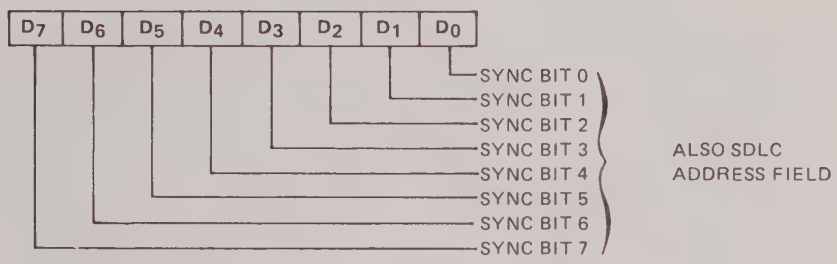

D7 D6 D5 D4 D3 D2 D1 D0
PARITY ENABLE
PARITY EVEN/ODD
0 0 SYNC MODES ENABLE
0 1 1 STOP BIT/CHARACTER
1 0 1 1/2 STOP BITS/CHARACTER
1 1 2 STOP BITS/CHARACTER
0 0 8 BIT SYNC CHARACTER
0 1 16 BIT SYNC CHARACTER
1 0 SDLC MODE (01111110 FLAG)
1 1 EXTERNAL SYNC MODE
0 0 X1 CLOCK MODE
0 1 X16 CLOCK MODE
1 0 X32 CLOCK MODE
1 1 X64 CLOCK MODE

WRITE REGISTER BIT FUNCTIONS (CONT.)

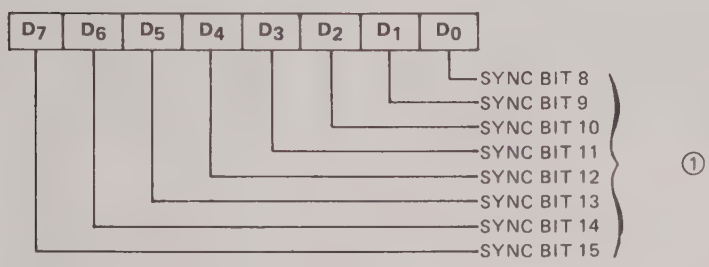
WRITE REGISTER 5



WRITE REGISTER 6

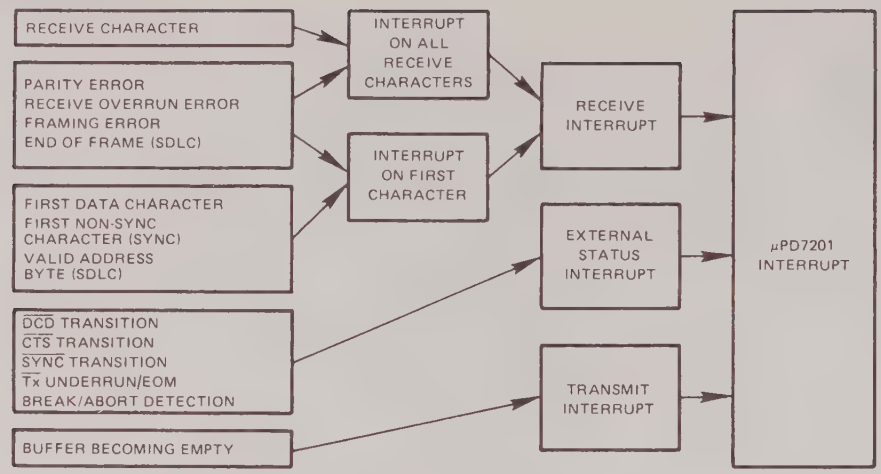


WRITE REGISTER 7



Note: ① For SDLC it must be programmed to "01111110" for flag recognition.

INTERRUPT STRUCTURE



WR2s BITS IN CH. A			PRIN	MODE	CONTENTS ON DATA BUS DRIVEN BY THE μPD7201 AT EACH INTA SEQUENCE		
					1st INTA	2nd INTA	3rd INTA (*)
D_5	D_4	D_3			D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
0	x	x	x	Non-vectored	High-Z	High-Z	High-Z
1	0	0	0	8085 Master	(Call) 1 1 0 0 1 1 0 1	V_7 V_6 V_5 V_4 V_3 V_2 V_1 V_0	0 0 0 0 0 0 0 0
1	0	0	1	8085 Master	1 1 0 0 1 1 0 1	High-Z	High-Z
1	0	1	0	8085 Slave	High-Z	V_7 V_6 V_5 V_4 V_3 V_2 V_1 V_0	0 0 0 0 0 0 0 0
1	0	1	1	8085 Slave	High-Z	High-Z	High-Z
1	1	0	0	8086	High-Z	V_7 V_6 V_5 V_4 V_3 V_2 V_1 V_0	
1	1	0	1	8086	High-Z	High-Z	

(*) 3rd $\overline{\text{INTA}}$ is 8085 Mode

Signetics

2672 Programmable Video Timing Controller (PVTC)

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PROGRAMMABLE VIDEO TIMING CONTROLLER (PVTC) 2672

PRELIMINARY SPECIFICATION

DESCRIPTION

The Signetics 2672 Programmable Video Timing Controller (PVTC) is a programmable device designed for use in CRT terminals and display systems that employ raster scan techniques. The PVTC generates the vertical and horizontal timing signals necessary for the display of interlaced or non-interlaced data on a CRT monitor. It provides consecutive addressing to a user specified display buffer memory domain and controls the CPU-display buffer interface for various buffer configuration modes. A variety of operating modes, display formats, and timing profiles can be implemented by programming the control registers in the PVTC.

A minimum CRT terminal system configuration consists of a PVTC, a 2671 Keyboard and Communication Controller (PKCC), a 2670 Display Character and Graphics Generator (DCGG), a 2673 Video and Attributes Controller (VAC), a single chip microcomputer such as the 8048, a display buffer RAM, and a small amount of TTL for miscellaneous address decoding, interface, and control. Typically, the package count for a minimum system is between 15 and 20 devices; system complexity can be enhanced by upgrading the microprocessor and expanding via the system address and data busses.

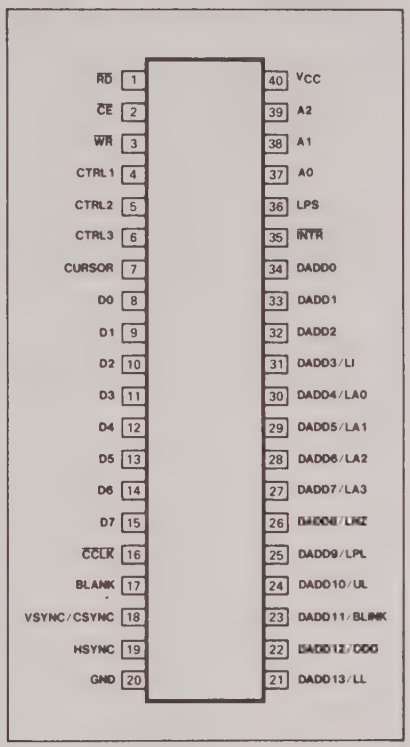
FEATURES

- 4MHz character rate
- Up to 256 characters per row
- 1 to 16 raster lines per character row
- Up to 128 character rows per frame
- Programmable horizontal and vertical sync generators
- Interlaced or non-interlaced operation
- Up to 16K RAM addressing for multiple page operation
- Automatic wraparound of RAM
- Addressable incrementable and readable cursor
- Programmable cursor size, position, and blink
- Split screen and horizontal scroll capability
- Light pen register
- Selectable buffer interface modes
- Dynamic RAM refresh
- Completely TTL compatible
- Single +5 volt power supply
- Power on reset circuit

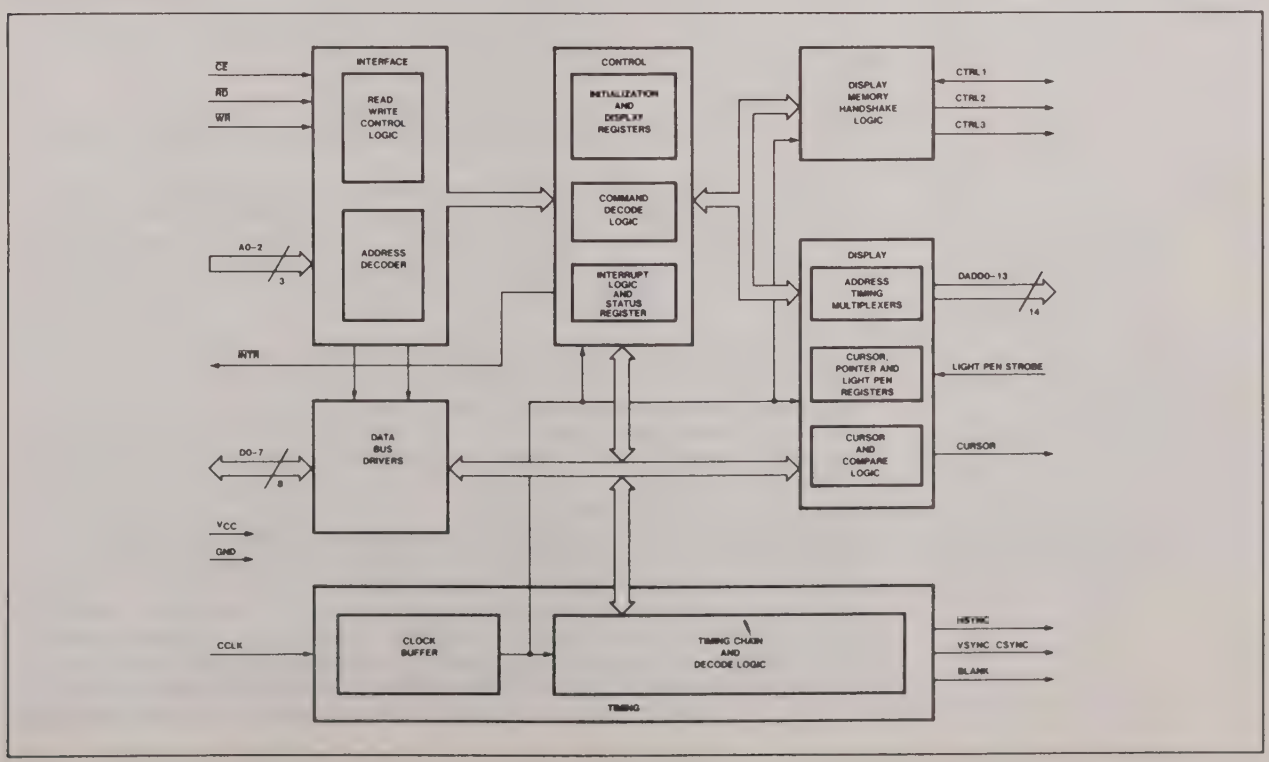
APPLICATIONS

- CRT terminals
- Word processing systems
- Small business computers
- Home Computers

PIN CONFIGURATION



BLOCK DIAGRAM



PROGRAMMABLE VIDEO TIMING CONTROLLER (PVTC) 2672

PRELIMINARY SPECIFICATION

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%, T_A = 0°C to 70°C
Ceramic DIP	2672I
Plastic DIP	2672N

PIN DESIGNATION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
A0–A2	37–39	I	**Address Lines:** Used to select PVTC internal registers for read/write operations and for commands.
D0–D7	8–15	I/O	**8-Bit Bidirectional Three-State Data Bus.** Bit 0 is the LSB and bit 7 is the MSB. All data, command, and status transfers between the CPU and the PVTC takeplace over this bus. The direction of the transfer is controlled by the $\overline{RD}$ and $\overline{WR}$ inputs when the $\overline{CE}$ input is low. When the $\overline{CE}$ input is high, the data bus is in the three-state condition.
$\overline{RD}$	1	I	**Read Strobe:** Active low input. A low on this pin while $\overline{CE}$ is low causes the contents of the register selected by A0–A2 to be placed on the data bus. The read cycle begins on the leading (falling) edge of $\overline{RD}$.
$\overline{WR}$	3	I	**Write Strobe:** Active low input. A low on this pin while $\overline{CE}$ is also low causes the contents of the data bus to be transferred to the register selected by A0–A2. The transfer occurs on the trailing (rising) edge of $\overline{WR}$.
$\overline{CE}$	2	I	**Chip Enable:** Active low input. When low, data transfers between the CPU and the PVTC are enabled on D0–D7 as controlled by the $\overline{WR}$, $\overline{RD}$, and A0–A2 inputs. When $\overline{CE}$ is high, the PVTC is effectively isolated from the data bus and D0–D7 are placed in the three-state condition.
$\overline{CCLK}$	16	I	**Character Clock:** Timing signal derived from the video dot clock which is used to synchronize the PVTC's timing functions.
HSYNC	19	O	**Horizontal Sync:** Active high output which provides video horizontal sync pulses. The timing parameters are programmable.
VSYNC/CSYNC	18	O	**Vertical Sync/Composite Sync:** A control bit selects either vertical or composite sync pulses on this active high output. When CSYNC is selected, equalization pulses are included. The timing parameters are programmable.
BLANK	17	O	**Blank:** This active high output defines the horizontal and vertical borders of the display. Display control signals which are output on DADD3 thru DADD13 are valid on the trailing edge of BLANK.
CURSOR	7	O	**Cursor Gate:** This active high output becomes active for a specified number of scan lines when the address contained in the cursor registers match the address output on DADD0 thru DADD13. The first and last lines of the cursor and a blink option are programmable.
$\overline{INTR}$	35	O	**Interrupt Request:** Open drain output which supplies an active low interrupt request from any of five maskable sources. This pin is inactive after power on reset or a master reset command.
LPS	36	I	**Light Pen Strobe:** Positive edge triggered input indicating a light pen hit. Causes the current value of the display address to be strobed into the light pen register.
CTRL1	4	I/O	**Handshake Control 1:** In independent mode, provides an active low write data buffer ($\overline{WDB}$) output which strobes data from the interface latch into the display memory. In transparent and shared modes, this is an active low processor bus request ($\overline{PBREQ}$) input which indicates that the CPU desires to access the display memory. This control output has no meaning in row buffer mode.
CTRL2	5	O	**Handshake Control 2:** In independent mode, provides an active low read data buffer ($\overline{RDB}$) output which strobes data from the display memory into the interface latch. In transparent and shared modes, this is an active low bus external enable ($\overline{BEXT}$) output which indicates that the PVTC has relinquished control of the display memory (DADD0–DADD13 are in the three-state condition) in response to a CPU bus request. $\overline{BEXT}$ also goes low in response to a 'display off and float DADD' command. In row buffer mode, it is an active low bus request ($\overline{BREQ}$) output which halts the CPU during a line DMA.

PIN DESIGNATION (cont.)

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
CTRL3	6	O	**Handshake Control 3:** In independent mode, provides the active low buffer chip enable ($\overline{BCE}$) signal to the display memory. In transparent and shared modes, provides an active low bus acknowledge ($\overline{BACK}$) output which serves as a ready signal to the CPU in response to a processor bus request. In row buffer mode, this is an active high memory bus control (MBC) output which configures the system for the DMA transfer of one row of character codes from system memory to the row display buffer.
DADD0–DADD13	34–21	O	**Display Address:** Used by the PVTC to address up to 16K of display memory. These outputs are floated at various times depending on the buffer mode. Various control signals are multiplexed on DADD3 thru DADD13 and are valid at the trailing edge of BLANK. These control signals are: **DADD3/LI** **Line Interlace:** Replaces DADD4/LA0 as the least significant line address for interlaced sync and video applications. A low indicates an even row of an even field or an odd row of an odd field. **DADD4–DADD7/LA0–LA3** **Line Address:** Provides the number of the current scan line within each character row. **DADD8/LNZ** **Line Zero:** Asserted before the first scan line in each character row. **DADD9/LPL** **Light Pen Line:** Asserted before the scan line which matches the programmed light pen line position (line 3, 5, 7, or 9). **DADD10/UL** **Underline:** Asserted before the scan line which matches the programmed underline position (line 0 thru 15). **DADD11/BLINK** **Blink frequency:** Provides an output divided down from the vertical sync rate. **DADD12/ODD** **Odd Field:** Active high signal which is asserted before each scan line of the odd field when interlace is specified. **DADD13/LL** **Last Line:** Asserted before the last scan line of each character row.
V_{CC}	40	I	**Power Supply:** +5 volts ± 5% power input.
GND	20	I	**Ground:** Signal and power ground input.

FUNCTIONAL DESCRIPTION

As shown on the block diagram, the PVTC contains the following major blocks:

- Data bus buffer
- Interface Logic
- Operation Control
- Timing
- Display Control
- Buffer Control

Data Bus Buffer

The data bus buffer provides the interface between the external and internal data busses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the PVTC.

Interface Logic

The interface logic contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer. The functions performed by the CPU read and write operations are as shown in table 1.

Table 1 PVTC ADDRESSING

A2	A1	A0	READ (RD=0)	WRITE (WR=0)
0	0	0	Interrupt register	Initialization registers[1]
0	0	1	Status register	Command register
0	1	0	Screen start address lower register	Screen start address lower reg.
0	1	1	Screen start address upper register	Screen start address upper reg.
1	0	0	Cursor address lower register	Cursor address lower register
1	0	1	Cursor address upper register	Cursor address upper register
1	1	0	Light pen address lower register	Display pointer address lower reg.
1	1	1	Light pen address upper register	Display pointer address upper reg.

NOTE

1. There are 11 initialization registers which are accessed sequentially via a single address. The PVTC maintains an internal pointer to these registers which is incremented after each write at this address until the last register (IR10, the split screen register) is accessed. The pointer then continues to point to the split screen register. Upon power–up or a master reset command, the internal pointer is reset to point to the first register (IR0) of the initialization register group. The internal pointer can also be preset to any register of the group via the 'load IR address pointer' command.

Operation Control

The operation control section decodes configuration and operation commands from the CPU and generates appropriate signals to other internal sections to control the overall device operation. It contains the timing and display registers which configure the display format and operating mode, the interrupt logic, and the status register which provides operational feedback to the CPU.

Timing

The timing section contains the counters and decoding logic necessary to generate the monitor timing outputs and to control the display format. These timing parameters are selected by programming of the initialization registers.

Display Control

The display control section generates linear addressing for up to 16K bytes of display memory. Internal comparators limit the portion of the memory which is displayed to programmed values. Additional functions performed in this section include cursor positioning, storage of light pen 'hit' location, and address comparisons required for generation of timing signals and the split screen interrupt.

Buffer Control

The buffer control section generates three signals which control the transfer of data between the CPU and the display buffer memory. Four system configurations requiring four different 'handshaking' schemes are supported. These are described below.

SYSTEM CONFIGURATIONS

Figure 1 illustrates the block diagram of a typical display terminal using the Signetics 2670, 2671, 2672, and 2673 CRT terminal devices. In this system, the CPU examines inputs from the data communications line and the keyboard and places the data to be displayed in the display buffer memory. This buffer is typically a RAM which holds the data for a single or multiple screenload (page) or for a single character row.

The PVTC supports four common system configurations of display buffer memory, designated the independent, transparent, shared, and row buffer modes. The first three modes utilize a single or multiple page RAM and differ primarily in the means used to transfer display data between the RAM and the CPU. The row buffer mode makes use of a single row buffer (which can be a shift register or a small RAM) that is updated in real time to contain the appropriate display data.

The user programs bits 0 and 1 of IR0 to select the mode best suited for the system environment. The CNTRL1–3 outputs perform different functions for each mode and are named accordingly in the description of each mode.

Independent Mode

The CPU to RAM interface configuration for this mode is illustrated in figure 2. Transfer of data between the CPU and display memory is accomplished via a bidirectional latched port and is controlled by the signals read data buffer ($\overline{RDB}$), write data buffer ($\overline{WDB}$), and buffer chip enable ($\overline{BCE}$). This mode provides a non–contention type of operation that does not require address multiplexers. The CPU does not address the memory directly—the read or write operation is performed at the address contained in the cursor address register or the pointer address register as specified by the CPU. The PVTC enacts the data transfers during blanking intervals in order to prevent visual disturbances of the displayed data.

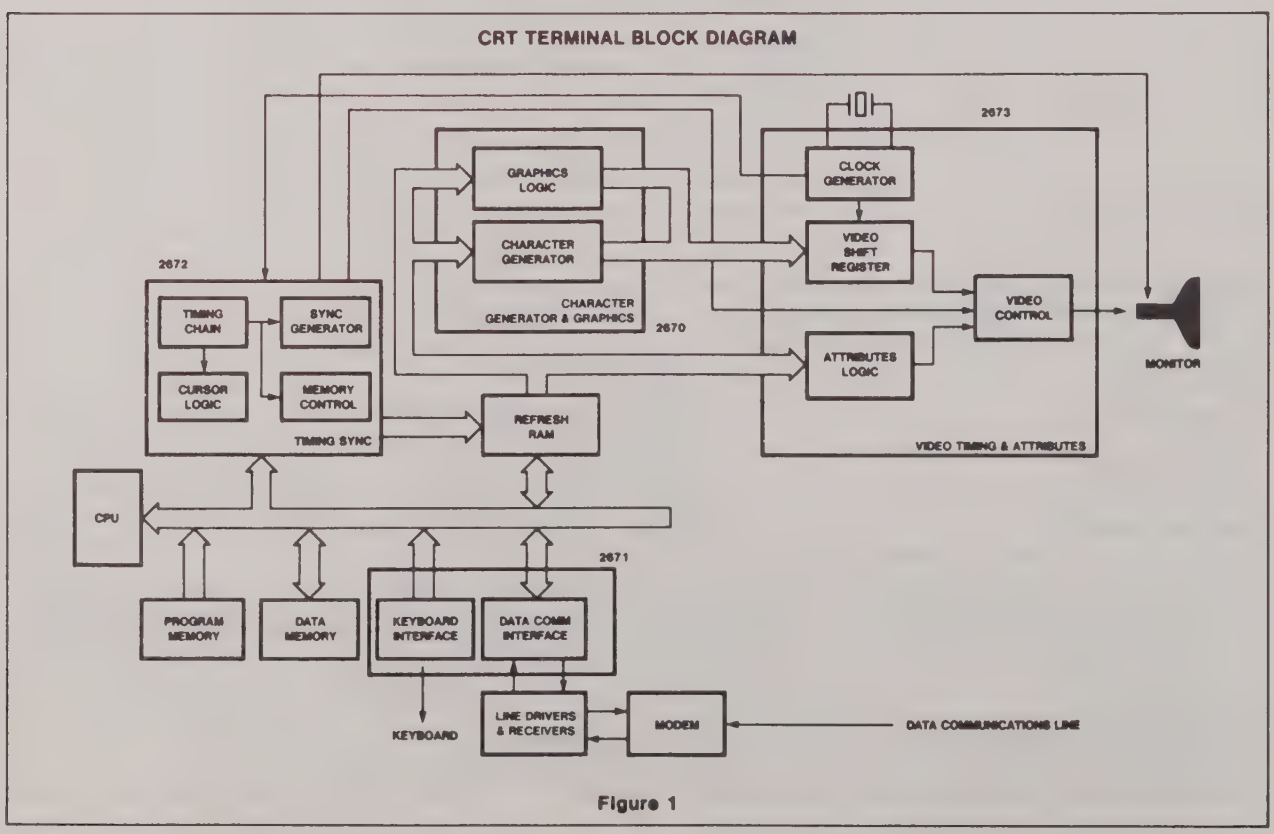


Figure 1

The CPU manages the data transfers by supplying commands to the PVTC. The commands used are:

1. Read/Write at pointer address.
2. Read/Write at cursor address (with optional increment of address).
3. Write from cursor address to pointer address.

The operational sequence for a write operation is:

1. CPU loads data to be written to display memory into the interface latch.
2. CPU writes address into cursor or pointer registers.
3. CPU checks RDFLG status bit to assure that any previous operation has been completed.
4. CPU issues 'write at cursor with/without increment' or 'write at pointer' command.
5. PVTC generates control signals and outputs specified address to perform requested operation. Data is copied from the interface latch into the memory.
6. PVTC sets RDFLG status to indicate that the write is completed.

Similarly, a read operation proceeds as follows:

1. Steps 2 and 3 as above.
2. CPU issues 'read at cursor with/without increment' or 'read at pointer' command.
3. PVTC generates control signals and outputs specified address to perform requested operation. Data is copied from memory to the interface latch and PVTC sets RDFLG status to indicate that the read is completed.
4. CPU checks RDFLG status to see if operation is completed.
5. CPU reads data from interface latch.

Loading the same data into a block of display memory is accomplished via the 'write from cursor to pointer' command:

1. CPU loads data to be written to display memory into the interface latch.
2. CPU writes beginning address of memory block into cursor address register and ending address of block into pointer address register.
3. CPU checks RDFLG status bit to assure that any previous operation has been completed.
4. CPU issues 'write from cursor to pointer' command.
5. PVTC generates control signals and outputs block addresses to copy data from the interface latch into the specified block of memory.
6. PVTC sets RDFLG status to indicate that the block write is completed.

Similar sequences can be implemented on an interrupt driven basis using the READY interrupt output to advise the CPU that a previously requested command has been completed.

Two timing sequences are possible for the 'read/write at cursor/pointer' commands. If the command is given during the active display window (defined as first scan line of the first character row to the last scan line of the last character row), the operation takes place during the next horizontal blanking interval, as illustrated in figure 3. If the command is given during the vertical blanking interval, or while the display has been commanded blanked, the operation takes place immediately. In the latter case, the execution time for the command is approximately one microsecond plus six (6) character clocks (see figure 4).

Timing for the 'write from cursor to pointer' operation is shown in figure 5. The BLANK output is asserted automatically and remains asserted until the vertical retrace interval following completion of the command. The memory is filled at a rate of one location per two character times, plus a small amount of overhead.

INDEPENDENT BUFFER MODE CONFIGURATION

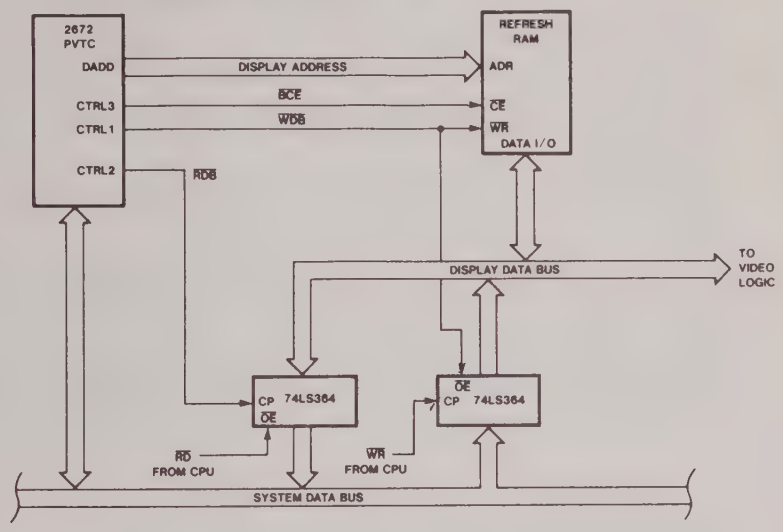
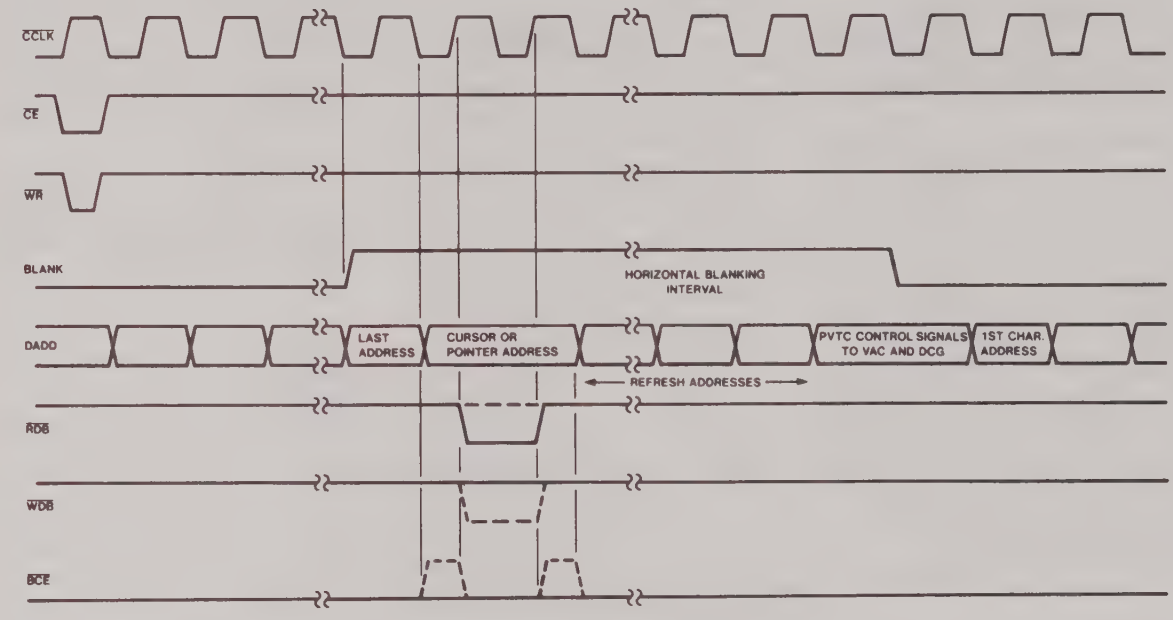


Figure 2

READ/WRITE AT CURSOR/POINTER COMMAND TIMING
(Command received during active display window)



NOTE
Write waveforms shown in dotted lines.

Figure 3

READ/WRITE AT CURSOR/POINTER COMMAND TIMING
(Command received while display is blanked)

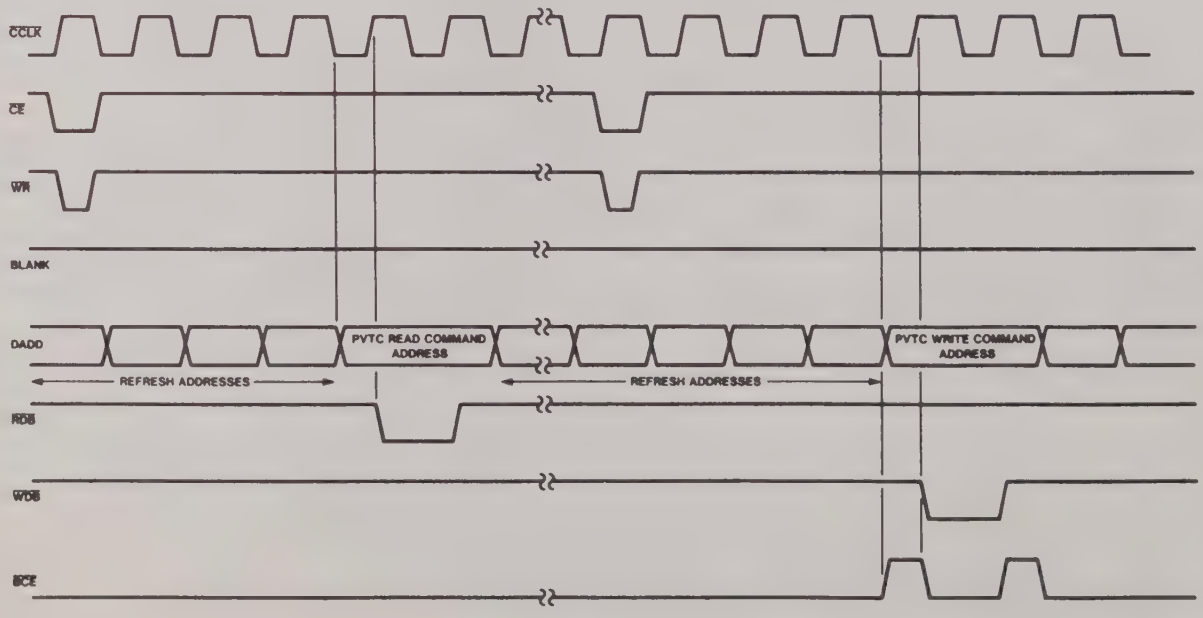


Figure 4

WRITE FROM CURSOR TO POINTER COMMAND TIMING

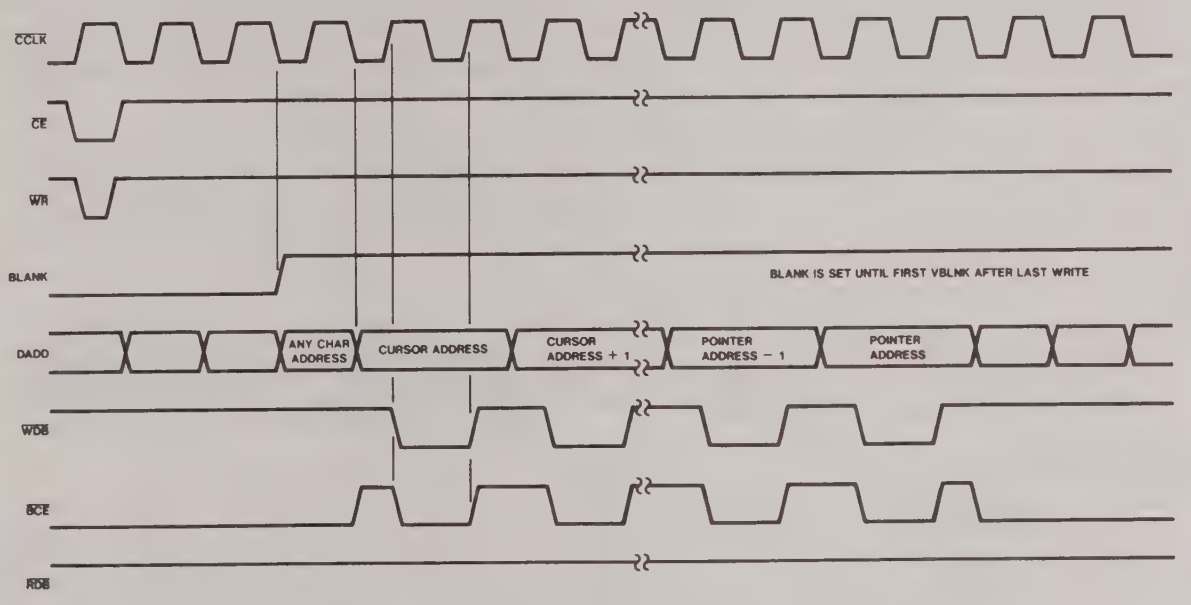


Figure 5

Shared and Transparent Buffer Modes

In these modes the display buffer RAM is a part of the CPU memory domain and is addressed directly by the CPU. Both modes use the same hardware configuration with the CPU accessing the display buffer via three−state drivers (see figure 6). The processor bus request ($\overline{PBREQ}$) control signal informs the PVTC that the CPU is requesting access to the display buffer. In response to this request, the PVTC raises bus acknowledge ($\overline{BACK}$) until its bus external ($\overline{BEXT}$) output has freed the display address and data busses for CPU access. $\overline{BACK}$, which can be used as a 'hold' input to the CPU, is then lowered to indicate that the CPU can access the buffer.

In transparent mode, the PVTC delays the granting of the buffer to the CPU until a vertical or horizontal blanking interval, thereby causing minimum disturbance of the display. In shared mode, the PVTC will blank the display and grant immediate access to the CPU. Timing for these modes is illustrated in figures 7, 8, and 9.

PVTC SHARED OR TRANSPARENT BUFFER MODES

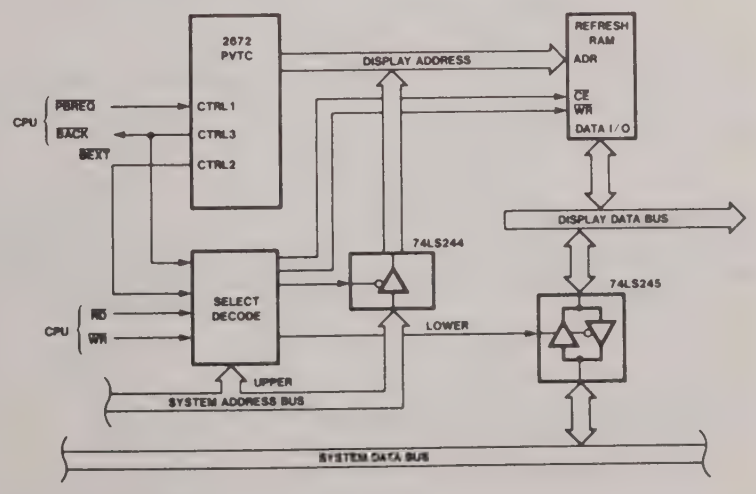
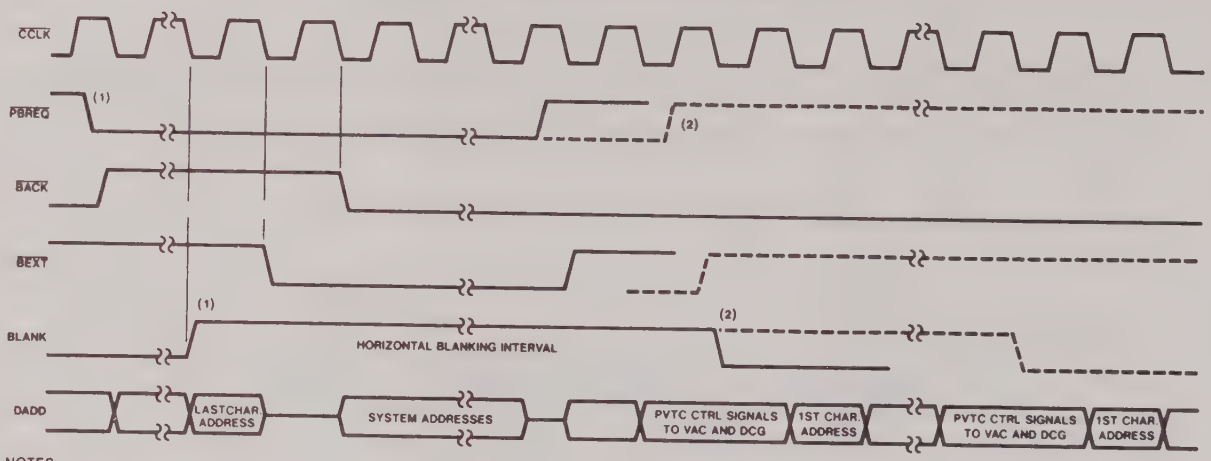


Figure 6

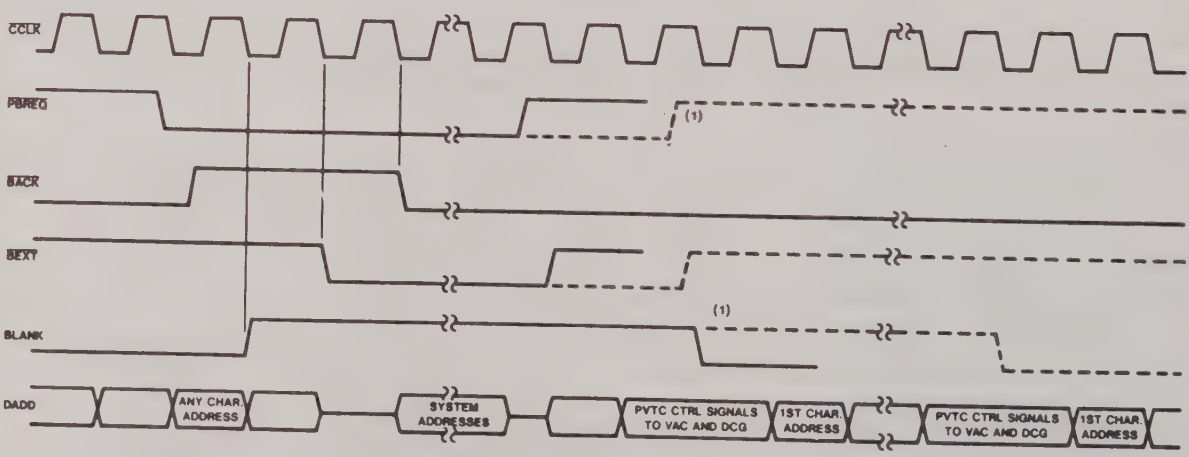
TRANSPARENT BUFFER MODE TIMING



NOTES
1. $\overline{\text{PBREQ}}$ must be asserted prior to the rising edge of BLANK in order for sequence to begin during that blanking period.
2. If $\overline{\text{PBREQ}}$ is negated after the next to last $\overline{\text{CCLK}}$ of the horizontal blanking interval, the next scan line will also be blanked.

Figure 7

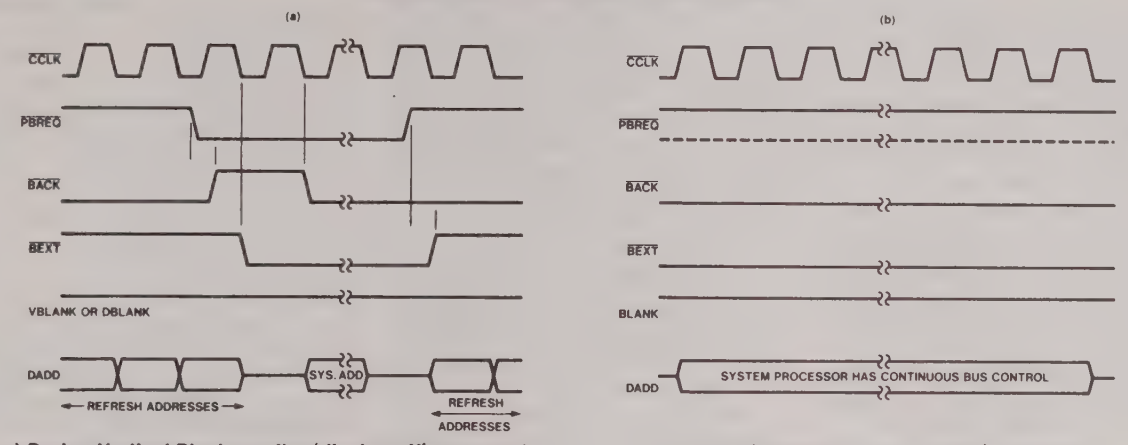
SHARED BUFFER MODE TIMING



NOTE
1. If $\overline{\text{PBREQ}}$ is negated after the next to last $\overline{\text{CCLK}}$ of the horizontal blanking interval, the next scan line will also be blanked.

Figure 8

SHARED AND TRANSPARENT MODE TIMING



a) During Vertical Blank or after 'display off' command

b) After 'display off and 3–state' command

Figure 9

Row Buffer Mode

Figure 10 and 11 show the timing and a typical hardware implementation for the row buffer mode. During the first scan line (line 0) of each character row, the PVTC halts the CPU and DMA's the next row of character data from the system memory to the row buffer memory. The PVTC then releases the CPU and displays the row buffer data for the programmed number of scan lines. The control signal $\overline{BREQ}$ informs the CPU that character addresses and the MBC signal will start at the next falling edge of BLANK. The CPU must release the address and data busses before this time to prevent bus contention. After the row of character data is transferred to the CPU, $\overline{BREQ}$ returns high to grant memory control back to the CPU.

ROW BUFFER MODE CONFIGURATION

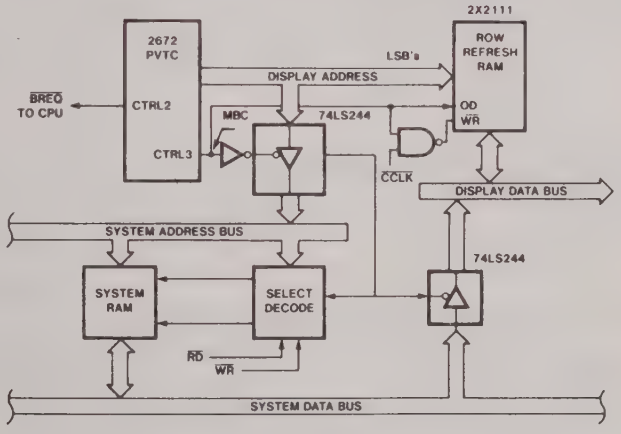


Figure 10

ROW BUFFER MODE TIMING

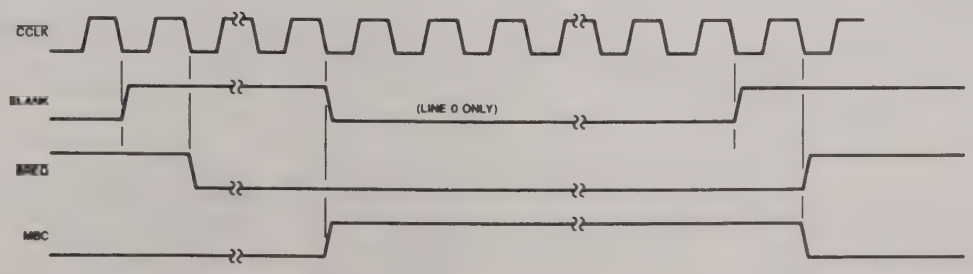


Figure 11

OPERATION

After power is applied, the PVTC will be in an inactive state. Two consecutive 'master reset' commands are necessary to release this circuitry and ready the PVTC for operation. Two register groups exist within the PVTC: the initialization registers and the display control registers. The initialization registers select the system configuration, monitor timing, cursor shape, display memory domain, and screen format. These are loaded first and normally require no modification except for certain special visual effects. The display control registers specify the memory address of the base character (upper left corner of screen), the cursor position, and the pointer address for independent memory access mode. These usually require modification during operation.

After initial loading of the two register groups, the PVTC is ready to control the monitor screen. Prior to executing the PVTC commands which turn on the display and cursor, the user should load the display memory with the first data to be displayed. During operation, the PVTC will sequentially address the display memory within the limits programmed into its registers. The memory outputs character codes to the system character and graphics generation logic, where they are converted to the serial video stream necessary to display the data on the CRT. The user effects changes to the display by modifying the contents of the display memory, the PVTC display control and command registers, and the initialization registers, if required. Interrupts and status conditions generated by the PVTC supply the 'handshaking' information necessary for the CPU to effect the display changes in the proper time frame.

INITIALIZATION REGISTERS

There are 11 initialization registers (IR0–IR10) which are accessed sequentially via a single address. The PVTC maintains an internal pointer to these registers which is incremented after each write at this address until the last register (IR10, the split screen register) is accessed. The pointer then continues to point to the split screen register. Upon power–up or a master reset command, the internal pointer is reset to point to the first register (IR0) of the initialization register group. The internal pointer can also be preset to any register of the group via the 'load IR address pointer' command. These registers are write only and are used to specify parameters such as the system configuration, display format, cursor shape, and monitor timing. Register formats are shown in figure 12.

INITIALIZATION REGISTER FORMATS

IR0

BIT7	BIT6 • BIT5 • BIT4 • BIT3		BIT2	BIT1 • BIT0
	SCAN LINES PER CHARACTER ROW		SYNC SELECT	BUFFER MODE SELECT
	NON-INTERLACED	INTERLACED		
NOT USED	0000 = 1 LINE 0001 = 2 LINES 0010 = 3 LINES • • 1110 = 15 LINES 1111 = 16 LINES	0000 = UNDEFINED 0001 = 5 LINES 0010 = 7 LINES • • 1110 = 31 LINES 1111 = UNDEFINED	0 = VSYNC 1 = CSYNC	00 = INDEPENDENT 01 = TRANSPARENT 10 = SHARED 11 = ROW

IR1

BIT7	BIT6 • BIT5 • BIT4 • BIT3 • BIT2 • BIT1 • BIT0
INTERLACE ENABLE	EQUALIZING CONSTANT
0 = NON-INT 1 = INTER.	000000 = 1 CCLK 000001 = 2 CCLK • • 111110 = 127 CCLK 111111 = 128 CCLK CALCULATED FROM: EC = 0.5(H_{ACT}+H_{FP}+H_{SYNC}+H_{BP}) − 2(H_{SYNC})

IR2

BIT7	BIT6 • BIT5 • BIT4 • BIT3	BIT2 • BIT1 • BIT0
	HORIZONTAL SYNC WIDTH	HORIZONTAL BACK PORCH
NOT USED	0000 = 2 CCLK 0001 = 4 CCLK • • 1110 = 30 CCLK 1111 = 32 CCLK	000 = 1 CCLK 001 = 5 CCLK • • 110 = 25 CCLK 111 = 29 CCLK

IR3

BIT7 • BIT6 • BIT5	BIT4 • BIT3 • BIT2 • BIT1 • BIT0
VERTICAL FRONT PORCH	VERTICAL BACK PORCH
000 = 4 SCAN LINES 001 = 8 SCAN LINES • • 110 = 28 SCAN LINES 111 = 32 SCAN LINES	00000 = 4 SCAN LINES 00001 = 6 SCAN LINES • • 11110 = 64 SCAN LINES 11111 = 66 SCAN LINES

IR4

BIT7	BIT6 • BIT5 • BIT4 • BIT3 • BIT2 • BIT1 • BIT0
CHARACTER BLINK RATE	ACTIVE CHARACTER ROWS PER SCREEN
0 = 1/16 VSYNC 1 = 1/32 VSYNC	0000000 = 1 ROW 0000001 = 2 ROWS • • 1111110 = 127 ROWS 1111111 = 128 ROWS

IR5

BIT7 • BIT6 • BIT5 • BIT4 • BIT3 • BIT2 • BIT1 • BIT0
ACTIVE CHARACTERS PER ROW
00000010 = 3 CHARACTERS 00000011 = 4 CHARACTERS = = 11111110 = 255 CHARACTERS 11111111 = 256 CHARACTERS

IR6

BIT7 • BIT6 • BIT5 • BIT4	BIT3 • BIT2 • BIT1 • BIT0
FIRST LINE OF CURSOR	LAST LINE OF CURSOR
000 = SCAN LINE 0 001 = SCAN LINE 1 • • 110 = SCAN LINE 14 111 = SCAN LINE 15	000 = SCAN LINE 0 001 = SCAN LINE 1 • • 110 = SCAN LINE 14 111 = SCAN LINE 15

IR7

BIT7 • BIT6	BIT5	BIT4	BIT3 • BIT2 • BIT1 • BIT0
LIGHT PEN LINE	CURSOR BLINK	DOUBLE HEIGHT CHAR.	UNDERLINE POSITION
00 = SCAN LINE 3 01 = SCAN LINE 5 10 = SCAN LINE 7 11 = SCAN LINE 9	0 = NO 1 = YES	0 = NO 1 = YES	0000 = SCAN LINE 0 0001 = SCAN LINE 1 • • 1110 = SCAN LINE 14 1111 = SCAN LINE 15

IR8

BIT7 • BIT6 • BIT5 • BIT4 • BIT3 • BIT2 • BIT1 • BIT0
DISPLAY BUFFER FIRST ADDRESS LSB'S
H'000 = 0 H'001 = 1 • • H'FFE = 4,094 H'FFF = 4,095 NOTE: MSB'S ARE IN IR9(3:0)

IR9

BIT7 • BIT6 • BIT5 • BIT4	BIT3 • BIT2 • BIT1 • BIT0
DISPLAY BUFFER LAST ADDRESS	DISPLAY BUFFER FIRST ADDRESS MSB'S
0000 = 1,023 0001 = 2,047 • • 1110 = 15,360 1111 = 16,383	SEE IR8

IR10

BIT7	BIT6 • BIT5 • BIT4 • BIT3 • BIT2 • BIT1 • BIT0
CURSOR BLINK RATE	SPLIT SCREEN INTERRUPT ROW
0 = 1/16 VSYNC 1 = 1/32 VSYNC	0000000 = ROW 0 0000001 = ROW 1 • • 1111110 = ROW 126 1111111 = ROW 127

Figure 12

IR0[6:3]—Scan Lines per Character Row

Both interlaced and non–interlaced scanning are supported by the PVTC. For interlaced mode, two different formats can be implemented, depending on the interconnection between the PVTC and the character generator (see IR1[7]). This field defines the number of scan lines used to compose a character row for each technique. As scanning occurs, the scan line count is output on the LA0–LA3 and LI pins.

IR0[2]—VS/CS Enable

This bit selects either vertical sync pulses or composite sync pulses on the VSYNC/CSYNC output (pin 18). The composite sync waveform conforms to EIA RS170 standards, with the vertical interval composed of six equalizing pulses, six vertical sync pulses, and six more equalizing pulses.

IR0[1:0]—Buffer Mode Select

Four buffer memory modes may be selectively enabled to accommodate the desired system configuration. See System Configuration.

IR1[7]—Interlace Enable

Specifies interlaced or noninterlaced timing operation. Two modes of interlaced operation are available, depending on whether L0–L3 or LI, L0–L2 are used as the line address for the character generator. The resulting displays are shown in figure 13.

For 'interlaced sync' operation, the same information is displayed in both odd and even fields, resulting in enhanced readability. The PVTC outputs successive line numbers in ascending order on the LA0–LA3 lines, one per scan line for each field.

The 'interlaced sync and video' format doubles the character density on the screen. The PVTC outputs successive line numbers in ascending order on the LI, LA0–LA2 lines, one per scan line for each field, but alternates beginning the count with even and odd line numbers. This displays the odd field with even scan lines in even character rows and odd scan lines in odd character rows, and the even field with odd scan lines in even character rows and even scan lines on odd character rows. This provides balanced beam currents in the odd and even fields, thus minimizing character variations due to different loading of the CRT anode supply between fields.

IR1[6:0]—Equalizing Constant

This field indirectly defines the horizontal front porch and is used internally to generate the equalizing pulses for the RS170 compatible CSYNC. The value for this field is the total number of character clocks ($\overline{CCLK}$) during a horizontal line period divided by two, minus two times the number of character clocks in the horizontal sync pulse:

$$EC = \frac{H_{ACT} + H_{FP} + H_{SYNC} + H_{BP}}{2} - 2(H_{SYNC})$$

The definition of the individual parameters is illustrated in figure 14.

Note that when using the 2673 VAC, it will delay the blank pulse three $\overline{CCLK}$s relative to the HSYNC pulse.

IR2[6:3]—Horizontal Sync Pulse Width

This field specifies the width of the HSYNC pulse in $\overline{CCLK}$ periods.

IR2[2:0]—Horizontal Back Porch

This field defines the number of CCLKs between the trailing edge of HSYNC and the trailing edge of BLANK.

IR3[7:5]—Vertical Front Porch

Programs the number of scan line periods between the rising edges of BLANK and VSYNC during a vertical retrace interval. The width of the VSYNC pulse is fixed at three scan lines.

IR3[4:0]—Vertical Back Porch

This field determines the number of scan line periods between the falling edges of the VSYNC and BLANK outputs.

IR4[7]—Character Blink Rate

Specifies the frequency for the character blink attribute timing. The blink rate can be specified as 1/16 or 1/32 of the vertical field rate. The timing signal has a duty cycle of 75% and is multiplexed onto the DADD11/BLINK output at the falling edge of each BLANK.

IR4[6:0]—Character Rows Per Screen

This field defines the number of character rows to be displayed. This value multiplied by the scan lines per character row, plus the vertical front and back porch values, and the vertical sync pulse width (three scan lines) is the vertical scan period in scan lines.

IR5[7:0]—Active Characters Per Row

This field determines the number of characters to be displayed on each row of the CRT screen. The sum of this value, the horizontal front porch, the horizontal sync width, and the horizontal back porch is the horizontal scan period in $\overline{CCLK}$s.

IR6[7:4], IR6[3:0]—First and Last Scan Line of Cursor

These two fields specify the height and position of the cursor on the character block. The 'first' line is the topmost line when scanning from the top to the bottom of the screen.

IR7[7:6]—Light Pen Line Position

This field defines which of four scan lines of the character row will be used for the light pen strike–thru attribute by the 2673 VAC. The timing signal is multiplexed onto the DADD9/LPL output during the falling edge of BLANK.

IR7[5]—Cursor Blink Enable

This bit controls whether or not the cursor output pin will be blinked at the selected rate (IR10[7]). The blink duty cycle for the cursor is 50%.

IR7[4]—Double Height Character Row Enable

If enabled, the number of each scan line will be repeated twice in succession, causing the height of the character row to double. This bit can be changed at any time but will only become effective at the beginning of the character row following the time it is changed. This allows selected character rows to be of double height. The split screen interrupt can be used to notify the CPU when to effectuate changes to this bit. For each double height row which replaces a normal row, one row count should be subtracted from the 'character rows per screen' field (IR4) to maintain the same total number of scan lines per field.

IR7[3:0]—Underline Position

This field defines which scan line of the character row will be used for the underline attribute by the 2673 VAC. The timing signal is multiplexed onto the DADD10/UL output during the falling edge of BLANK.

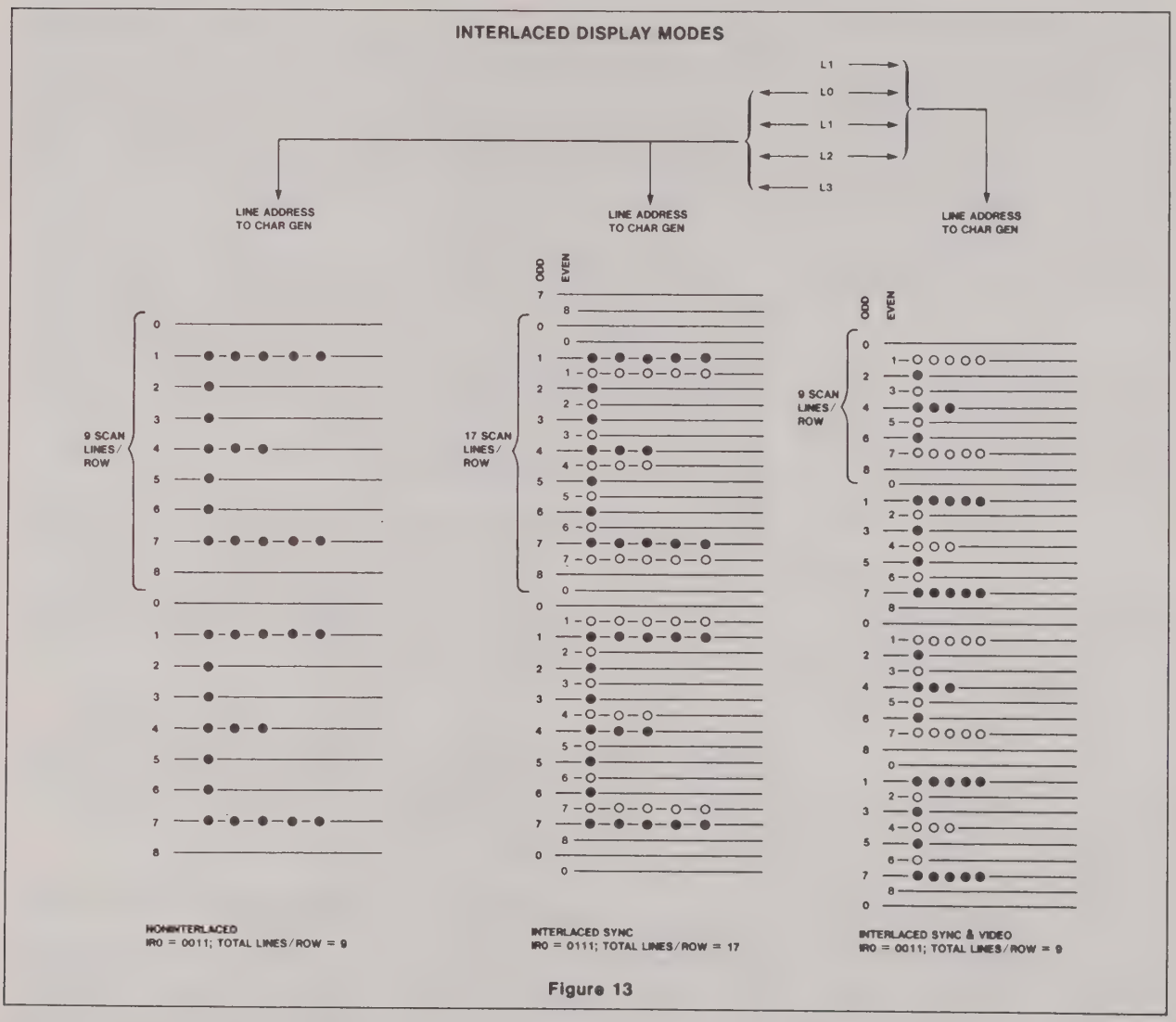


Figure 13

IR9[3:0], IR8[7:0]—Display Buffer First Address
IR9[7:4]—Display Buffer Last Address

These two fields define the area within the buffer memory where the display data will reside. When the data at the 'display buffer last address' is displayed, the PVTC will wrap—around and obtain the data to be displayed at the next screen position from the 'display buffer first address'. If 'last address' is the end of a character row and a new screen start address has been loaded into the screen start register, or if 'last address' is the last character position of the screen, the next data is obtained from the address contained in the screen start register.

Note that there is no restriction in displaying data from other areas of the addressable memory. Normally, the area between these two bounds is used for data which can be overwritten (e.g., as a result of scrolling), while data that is not to be overwritten would be contained outside these bounds and accessed by means of the split screen interrupt feature of the PVTC.

IR10[7] – Cursor Blink Rate

The cursor blink rate can be specified at 1/16 or 1/32 of the vertical scan frequency. Blink is effective only if blink is enabled by IR7[5].

IR10[6:0]—Split Screen Interrupt

The split screen interrupt can be used to provide special screen effects such as a row of double height characters or to change the normal addressing sequence of the display memory. The contents of this field is compared, in real time, to the current character row number. Upon a match, the PVTC sets the split screen status bit, and issues an interrupt request if so programmed. The status change/interrupt request is made at the beginning of scan line zero of the split screen character row.

HORIZONTAL AND VERTICAL TIMING

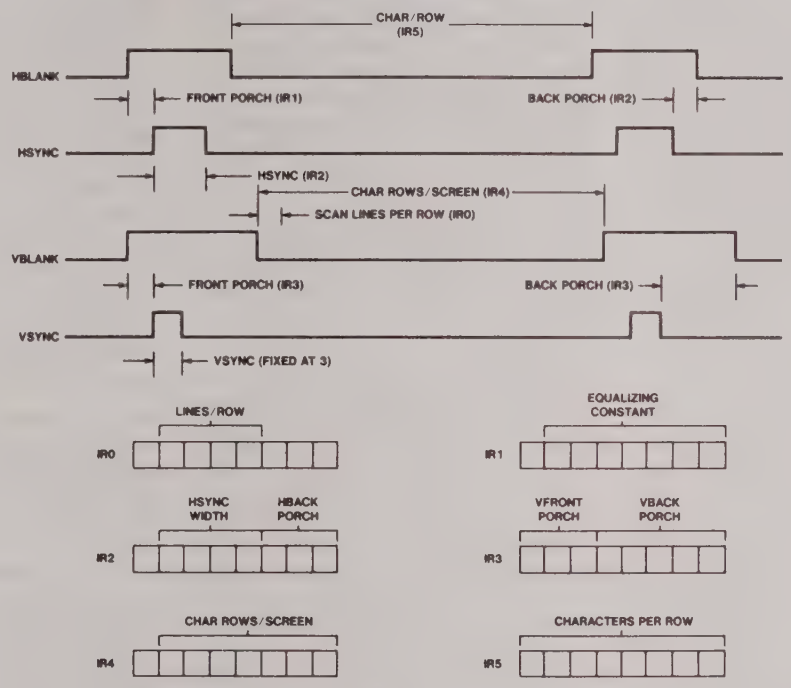


Figure 14

Timing Considerations

Normally, the contents of the initialization registers are not changed during operation. However, this may be necessary to implement special display features such as multiple cursors, smooth scrolling, horizontal scrolling, and double height character rows. Table 2 describes timing details for these registers which should be considered when implementing these features.

Table 2 TIMING CONSIDERATIONS

PARAMETER	TIMING CONSIDERATIONS
First line of cursor Last line of cursor Light pen line Underline	These parameters must be established at a minimum of two character times prior to their occurence.
Double height characters	Set/reset during the character row prior to the row which is to be/not to be double height
Cursor blink Cursor blink rate Character blink rate	New values become effective within one field after values are changed
Split screen interrupt row	Change anytime prior to line zero of desired row
Character rows per screen	Change only during vertical blanking period
Vertical front porch	Change prior to first line of V_{FP}
Vertical back porch	Change prior to fourth line after V_{SYNC}
Screen start register	Change prior to the horizontal blanking interval of the last line of character row before row where new value is to be used

DISPLAY CONTROL REGISTERS

There are nine registers in this group, each with an individual address. Their formats are illustrated in figure 15. The command register is used to invoke one of 16 possible PVTC commands as described in the COMMANDS section of this data sheet. The remaining registers in the group store address values which specify the cursor and buffer pointer locations, the location of the first character to be displayed on the screen, and the location of a light pen 'hit'. With the exception of the light pen register, the user initializes these registers after powering on the system and changes their values to control the data which is displayed.

Screen Start Registers

The screen start registers contain the address of the first character of the first row (upper left corner of the active display). At the beginning of the first scan line of the first row, this address is transferred to the row start register (RSR) and into the memory address counter (MAC). The counter is then advanced sequentially at the character rate the number of times programmed into the active characters per row register (IR5), thus reaching the address of the last character of the row plus one. At the beginning of each subsequent scan line of the first row, the MAC is reloaded from the RSR and the above sequence is repeated. At the end of the last scan line of the first row, the contents of the MAC is loaded into the RSR to serve as the starting memory address for the second character row. This process is repeated for the programmed number of rows per screen. Thus, the data in the display memory is displayed sequentially starting from the address contained in the screen start register. After the ensuing vertical retrace interval, the entire process repeats again.

The sequential operation described above will be modified upon the occurence of either of two events. First, if during the incrementing of the memory address counter the 'display buffer last address' (IR9[7:4]) is reached, the MAC will be loaded from the 'display buffer first address' register (IR9[3:0], IR8[7:0]) at the next character clock. Sequential operation will then resume starting from this address. This wraparound operation allows portions of the display buffer to be used for purposes other than storage of displayable data and is completely automatic without any CPU intervention (see figure 16a).

The sequential row to row addressing can also be modified under CPU control. If the contents of the screen start register (upper, lower, or both) are changed during any character row (say row 'n'), the starting address of the next character row (row 'n + 1') will be the new value of the screen start register and addressing will continue sequentially from there. This allows features such as split screen operation, partial scroll, or status line display to be implemented. The split screen interrupt feature of the PVTC is useful in controlling this type of operation. Note that in order to obtain the correct screen display, the screen start register must be reloaded with the original value prior to the end of the vertical retrace. See figure 16b.

During vertical blanking the address counter operation is modified by stopping the automatic load of the contents of the RSR into the counter, thereby allowing the address outputs to free–run. This allows dynamic memory refresh to occur during the vertical retrace interval. The refresh addressing starts at the last address displayed on the screen and increments by one for each character clock during the retrace interval. If the display buffer last address is encountered, refreshing continues from the display buffer first address.

Cursor Address Registers

The contents of these registers defines the buffer memory address of the cursor. If enabled, the cursor output will be asserted when the memory address counter matches the value of the cursor address registers. The cursor address registers may be read or written by the CPU or incremented via the 'increment cursor address' command. In independent buffer mode, these registers define a buffer memory address for PVTC controlled access in response to 'read/write at cursor with/without increment' commands, or the first address to be used in executing the 'write from cursor to pointer' command.

Display Pointer Address Registers

These registers define a buffer memory address for PVTC controlled accesses in response to 'read/write at pointer' commands. They also define the last buffer memory address to be written for the 'write from cursor to pointer' command.

Light Pen Address Registers

If the light pen input is enabled, these registers are used to store the current character address upon receipt of a light pen strobe input. Several sources of delay between the display of a character upon the screen and the receipt of a light pen hit can be expected to exist in a system environment. These delays include address pipelining in the character generation circuits, delays in the video generation circuits, and delays in the light detection circuitry itself. These delays cause the value stored in the light pen register to differ from the actual address of the character at which the light pen hit actually was detected. Software must be used to correct this condition.

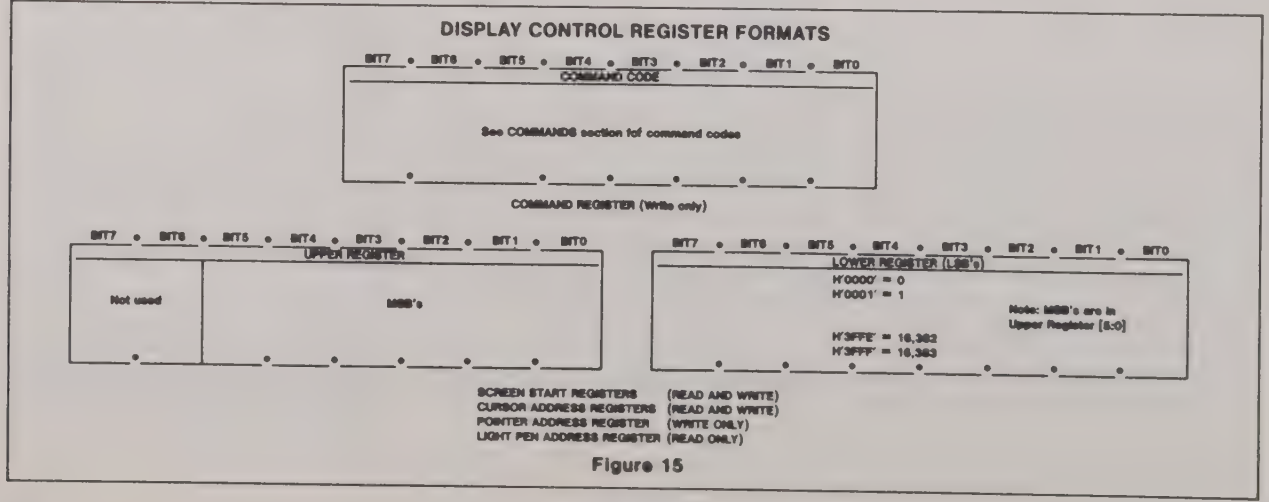

DISPLAY CONTROL REGISTER FORMATS
BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0
COMMAND CODE
See COMMANDS section for command codes
COMMAND REGISTER (Write only)
UPPER REGISTER
Not used
MSB's
LOWER REGISTER (LSB's)
H'0000' = 0
H'0001' = 1
Note: MSB's are in Upper Register [5:0]
H'3FFE' = 16,382
H'3FFF' = 16,383
SCREEN START REGISTERS (READ AND WRITE)
CURSOR ADDRESS REGISTERS (READ AND WRITE)
POINTER ADDRESS REGISTER (WRITE ONLY)
LIGHT PEN ADDRESS REGISTER (READ ONLY)

Figure 15

INTERRUPT/STATUS REGISTERS

The interrupt and status registers provide information to the CPU to allow it to interact with the PVTC to effect desired changes to implement various display operations. The interrupt register provides information on five possible interrupting conditions, as shown in figure 17. These conditions may be selectively enabled or disabled (masked) from causing interrupts by certain PVTC commands. An interrupt condition which is enabled (mask bit equal to one) will cause the $\overline{INTR}$ output to be asserted and will cause the corresponding bit in the interrupt register to be set upon occurrence of the interrupting condition. An interrupt condition which is disabled (mask bit equal to zero) has no effect on either the $\overline{INTR}$ output or the interrupt register.

The status register provides six bits of status information: the five possible interrupting conditions plus the NOT BUSY bit. For this register, however, the contents are not effected by the state of the mask bits.

Descriptions of each interrupt/status register bit follow. Unless otherwise indicated, a bit, once set, will remain set until reset by the CPU by issuing a 'reset interrupt/status bits' command. The bits are also reset by a 'master reset' command and upon power–up.

SR[5] – RDFLG

This bit is present in the status register only. A zero indicates that the PVTC is currently executing the previously issued command. A one indicates that the PVTC is ready to accept a new command.

I/SR[4] – VBLANK

Indicates the beginning of a vertical blanking interval. Is set to a one at the beginning of the first scan line of the vertical front porch.

I/SR[3] – Line Zero

Is set to a one at the beginning of the first scan line (line 0) of each active character row.

I/SR[2] – Split Screen

This bit is set when a match occurs between the current character row number and the value contained in the split screen interrupt register, IR10[6:0]. The equality condition is only checked at the beginning of line zero of each character row. This bit is reset when either of the screen start registers is loaded by the CPU.

I/SR[1] – Ready

Certain PVTC commands affect the display and may require the PVTC to wait for a blanking interval before enacting the command. This bit is set to one when execution of the command has been completed. No command should be invoked until the prior command is completed.

I/SR[0] – Light Pen

A one indicates that a light pen hit has occurred and that the contents of the light pen register have been updated. This bit will be reset when either of the light pen registers is read.

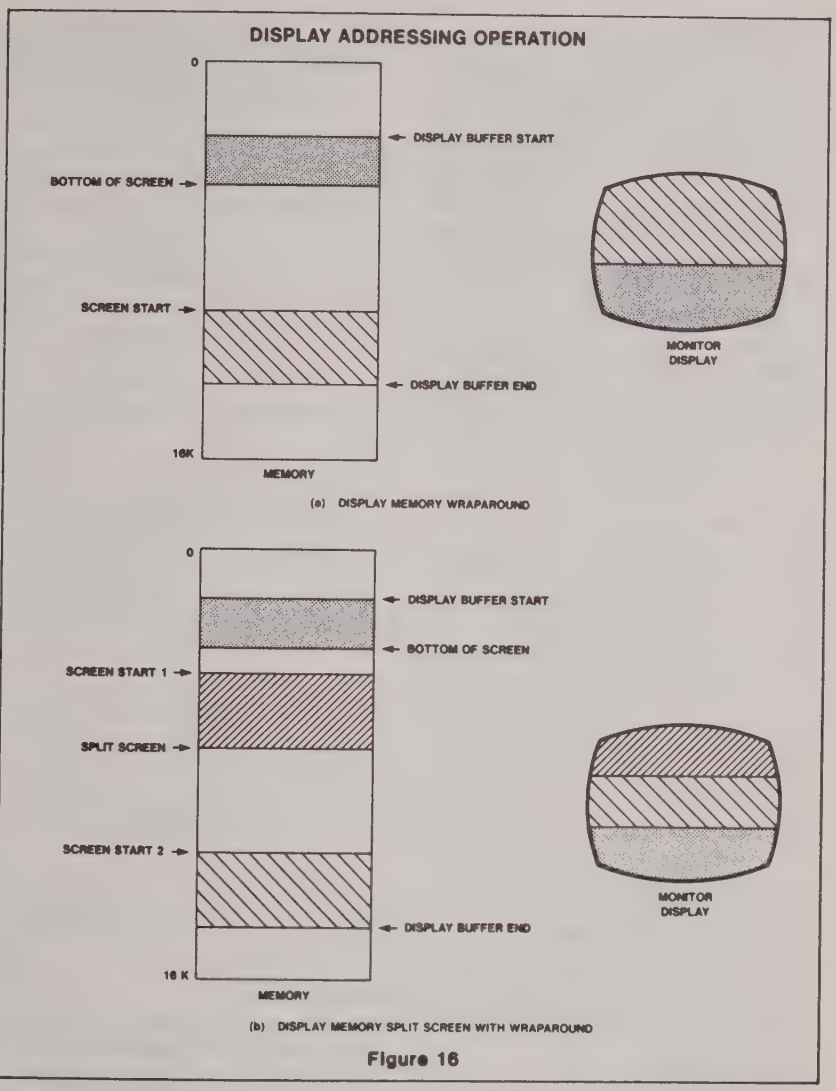


Figure 16

INTERRUPT AND STATUS REGISTER FORMAT

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		RDFLG	VBLANK	LINE ZERO	SPLIT SCREEN	READY	LIGHT PEN
Not used always read as 0		0 = Busy 1 = Ready	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Busy 1 = Ready	0 = No 1 = Yes

NOTE
*Status register only. Always 0 when reading interrupt register.

Figure 17

COMMANDS

The PVTC commands are divided into two classes: the instantaneous commands, which are executed immediately after they are invoked, and the delayed commands which may need to wait for a blanking interval prior to their execution. Command formats are shown in table 3. The commands are asserted by performing a write operation to the command register with the appropriate bit pattern as the data byte.

Instantaneous Commands

The instantaneous commands are executed immediately after the trailing edge of the $\overline{WR}$ pulse during which the command is issued. These commands do not affect the state of the RDFLG or READY interrupt/status bits. However, a command should not be invoked if the RDFLG bit is low.

Master Reset

This command initializes the PVTC and may be invoked at any time to return the PVTC to its initial state. Upon power–up, two successive master reset commands must be applied to release the PVTC's internal power on circuits. In transparent and shared buffer modes, the CNTRL1 input must be high when the command is issued. The command causes the following:

1. VSYNC and HSYNC go low and BLANK goes high. Scanning of the display will not begin until a 'display on' command is received.
2. The interrupt and status bits and masks are set to zero, except for the RDFLG flag which is set to a one.
3. The transparent mode, cursor off, display off, and light pen disable states are set.
4. The initialization register pointer is set to address IR0.

Load IR Address

This command is used to preset the initialization register pointer with the value 'V' defined by D3–D0. Allowable values are 0 to 10.

Enable Light Pen

After invoking this command, receipt of a light pen strobe input will cause the light pen register to be loaded with the current buffer memory address and the corresponding interrupt and status flag to be set. Once loaded, further loads are inhibited until either one of the light pen registers are read or a reset function is performed.

Disable Light Pen

Light pen hits will not be recognized.

Display Off

Asserts the BLANK output. The DADD0 thru DADD13 display address bus outputs may be optionally placed in the three–state condition by setting bit 2 to a '1' when invoking the command.

Table 3. PVTC Command Formats

D7	D6	D5	D4	D3	D2	D1	D0	Hex	COMMAND
Instantaneous Commands:									
0	0	0	0	0	0	0	0		Master reset
0	0	0	1	V	V	V	V		Load IR pointer with value V (V = 0 to 10)
0	0	1	d	d	d	1	0[1]		Disable light pen
0	0	1	d	d	d	1	1[2]		Enable light pen
0	0	1	d	1	N	d	0[1]		Display off. Float DADD bus if N = 1
0	0	1	d	1	N	d	1[2]		Display on: Next field (N = 1) or scan line (N = 0)
0	0	1	1	d	d	d	0[1]		Cursor off
0	0	1	1	d	d	d	1[2]		Cursor on
0	1	0	N	N	N	N	N		Reset interrupt/status: Bit reset where N = 1
1	0	0	N	N	N	N	N		Disable interrupt: Disable where N = 1
0	1	1	N	N	N	N	N		Enable interrupt: Enables interupts and resets the corresponding interrupt/status bits where N = 1
Delayed Commands:									
1	0	1	0	0	1	0	0	A4	Read at pointer address
1	0	1	0	0	0	1	0	A2	Write at pointer address
1	0	1	0	1	0	0	1	A9	Increment cursor address
1	0	1	0	1	1	0	0	AC	Read at cursor address
1	0	1	0	1	0	1	0	AA	Write at cursor address
1	0	1	0	1	1	0	1	AD	Read at cursor address and increment address
1	0	1	0	1	0	1	1	AB	Write at cursor address and increment address
1	0	1	1	1	0	1	1	BB	Write from cursor address to pointer address

NOTES
1. Any combination of these three commands is valid.
2. Any combination of these three commands is valid.
3. d = don't care.

Display On

Restores normal blanking operation either at the beginning of the next field (bit 2 = 1) or at the beginning of the next scan line (bit 2 = 0). Also returns the DADD0–DADD13 drivers to their active state.

Cursor Off

Disables cursor operation. Cursor output is placed in the low state.

Cursor On

Enables normal cursor operation.

Reset Interrupt/Status Bits

This command resets the designated bits in the interrupt and status registers. The bit positions correspond to the bit positions in the registers:

Bit 0 – Light pen
Bit 1 – Ready
Bit 2 – Split screen
Bit 3 – Line zero
Bit 4 – Vertical blank

Disable Interrupts

Sets the interrupt mask to zeros for the designated conditions, thus disabling these conditions from asserting the $\overline{INTR}$ output. Bit position correspondence is as above.

Enable Interrupts

Resets the selected interrupt and status register bits and writes the associated interrupt mask bits to a one. This enables the corresponding conditions to assert the $\overline{INTR}$ output. Bit position correspondence is as above.

Delayed Commands

This group of commands is utilized for the independent buffer mode of operation, although the 'increment cursor' command can also be used in other modes. With the exception of the 'write from cursor to pointer' and 'increment cursor' commands, all the commands of this type will be executed immediately or will be delayed depending on when the command is invoked. If invoked during the active screen time, the command is executed at the next horizontal blanking interval. If invoked during a vertical retrace interval or a 'display off' state, the command is executed immediately.

The 'increment cursor' and 'write from cursor to pointer' commands are executed immediately after they are issued. 'Increment cursor' requires approximately three $\overline{CCLK}$ periods for completion. 'Write from cursor to pointer' asserts the BLANK output during its execution. BLANK will not be released until the beginning of the vertical blanking interval following the last write operation. A second 'write from cursor to pointer' command should not be issued until this time.

In all cases, the PVTC will assert the READY/RDFLG status to signify completion of the command. No other commands should be given until the current command is completed. Therefore, the READY interrupt or RDFLG status flag should be used for handshaking control between the PVTC and CPU when using these commands.

Read/Write at Pointer
Transfers data between the display buffer and the bus interface latch using the address contained in the pointer register.

Read/Write at Cursor
Transfers data between the display buffer and the bus interface latch using the address contained in the cursor register.

Increment Cursor
Adds one (modulo 16K) to the cursor address register.

Read/Write at Cursor and Increment
Transfers data between the display buffer and the bus interface latch using the address contained in the cursor register and then adds one (modulo 16K) to the cursor address register.

Write from Cursor to Pointer
Writes the data contained in the bus interface latch into the block of display memory designated by the the cursor address and pointer address registers, inclusive. After completion of the command, the pointer address will be unchanged, but the cursor register contents will be equal to the pointer address.

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
Operating ambient temperature[2]	0 to +70	°C
Storage temperature	−65 to +150	°C
All voltages with respect to ground[3]	−0.5 to +6.0	V

DC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0\ V \pm 5\%$[4,5,6]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage		2.0			V
V_{OL}	Output low voltage	$I_{OL} = 1.6mA$			0.4	V
V_{OH}	Output high voltage (except $\overline{INTR}$ output)	$I_{OH} = -100\ uA$	2.4			V
I_{IL}	Input leakage current	$V_{IN} = 0$ to V_{CC}	−10		10	μA
I_{LL}	Data bus 3-state leakage current	$V_O = 0$ to V_{CC}	−10		10	μA
I_{OD}	$\overline{INTR}$ open drain output leakage current	$V_O = 0$ to V_{CC}			10	μA
I_{CC}	Power supply current				160	mA

NOTES
See next page.

AC ELECTRICAL CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5.0V + 5%[4,5,6,7,8]

PARAMETER		TEST CONDITIONS	TENTATIVE LIMITS			UNIT
			Min	Typ	Max	
Bus Timing (Fig. 18)[9]						
t_{AS}	A0–A2 setup time to $\overline{WR}$, $\overline{RD}$ low		30			ns
t_{AH}	A0–A2 hold time from $\overline{WR}$, $\overline{RD}$ high		0			ns
t_{CS}	$\overline{CE}$ setup time to $\overline{WR}$, $\overline{RD}$ low		0			ns
t_{CH}	$\overline{CE}$ hold time from $\overline{WR}$, $\overline{RD}$ high		0			ns
t_{RW}	$\overline{WR}$, $\overline{RD}$ pulse width		250			ns
t_{DD}	Data valid after $\overline{RD}$ low				200	ns
t_{DF}	Data bus floating after $\overline{RD}$ high				100	ns
t_{DS}	Data setup time to $\overline{WR}$ high		150			ns
t_{DH}	Data hold time from $\overline{WR}$ high		0			ns
t_{CC}	Time between READs and/or WRITEs[10]		600			ns
$\overline{CCLK}$ Timing (Fig. 19)						
t_{CCP}	$\overline{CCLK}$ period		250			ns
t_{CCH}	$\overline{CCLK}$ high time		100			ns
t_{CCL}	$\overline{CCLK}$ low time		100			ns
t_{CCD}	Output delay from $\overline{CCLK}$ edge				150	ns
Other Timings (Fig. 20)						
t_{RDL}	READY/RDFLG low from $\overline{WR}$ high[9]				t_{CCP} +30	ns
t_{BAK}	$\overline{BACK}$ high from $\overline{PBREQ}$ low				150	ns
t_{BXT}	$\overline{BEXT}$ high from $\overline{PBREQ}$ high				150	ns
t_{LPS}	Light pen strobe setup time to $\overline{CCLK}$ low		120			ns
t_{LPH}	Light pen strobe hold time from $\overline{CCLK}$ low		−10			ns
t_{IRL}	$\overline{INTR}$ low from $\overline{CCLK}$ low				150	ns
t_{IRH}	$\overline{INTR}$ high from $\overline{WR}$, $\overline{RD}$ high[9]				600	ns

Notes:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature and thermal resistance of 55°C/W junction to ambient (IWA ceramic package).
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range.
5. All voltage measurements are referenced to ground (GND).
6. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
7. For testing, all input signals swing between 0.4V and 2.4V with a transition time of 20ns maximum. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V as appropriate.
8. Test condition for outputs: C_L = 150pF.
9. Timing is illustrated and specified referenced to $\overline{WR}$ and $\overline{RD}$ inputs. Device may also be operated with $\overline{CE}$ as the 'strobing' input. In this case, all timing specifications apply referenced to falling and rising edges of $\overline{CE}$.
10. 1 microsecond minimum after 'master reset' command.

BUS TIMING

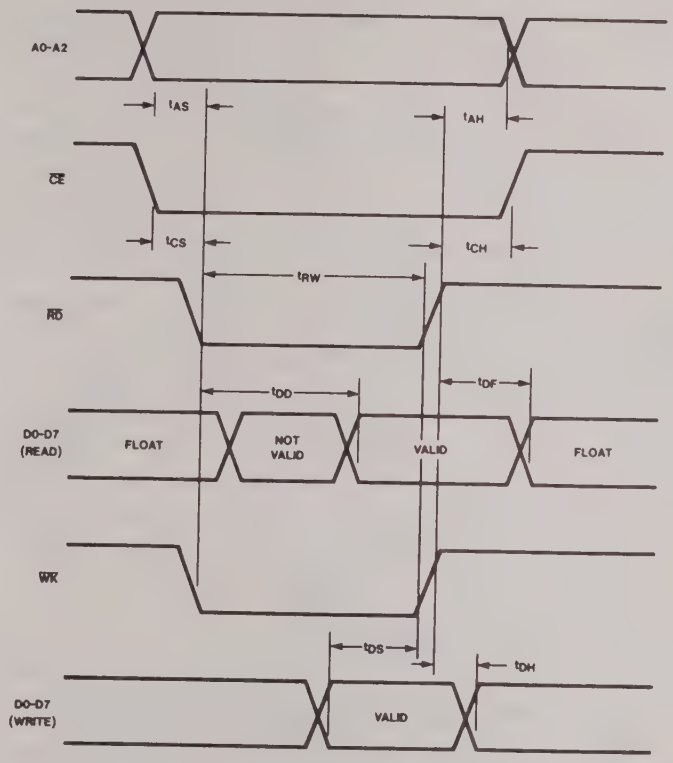
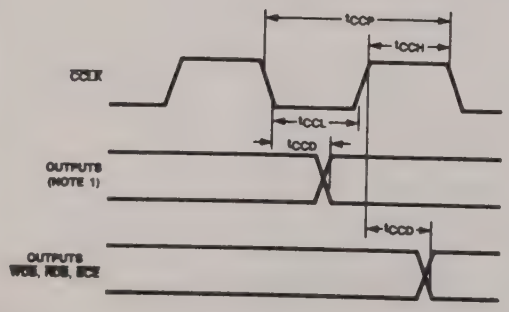


Figure 18

CCLK TIMING



NOTES
1. DADD0-DADD13, BLANK, HSYNC, CSYNC/VSYNC, CURSOR, $\overline{BEXT}$, $\overline{BREQ}$, $\overline{BCE}$, MBC, BACK
2. $\overline{BCE}$ changes state on both $\overline{CCLK}$ edges—(see Figures 3 and 4).

Figure 19

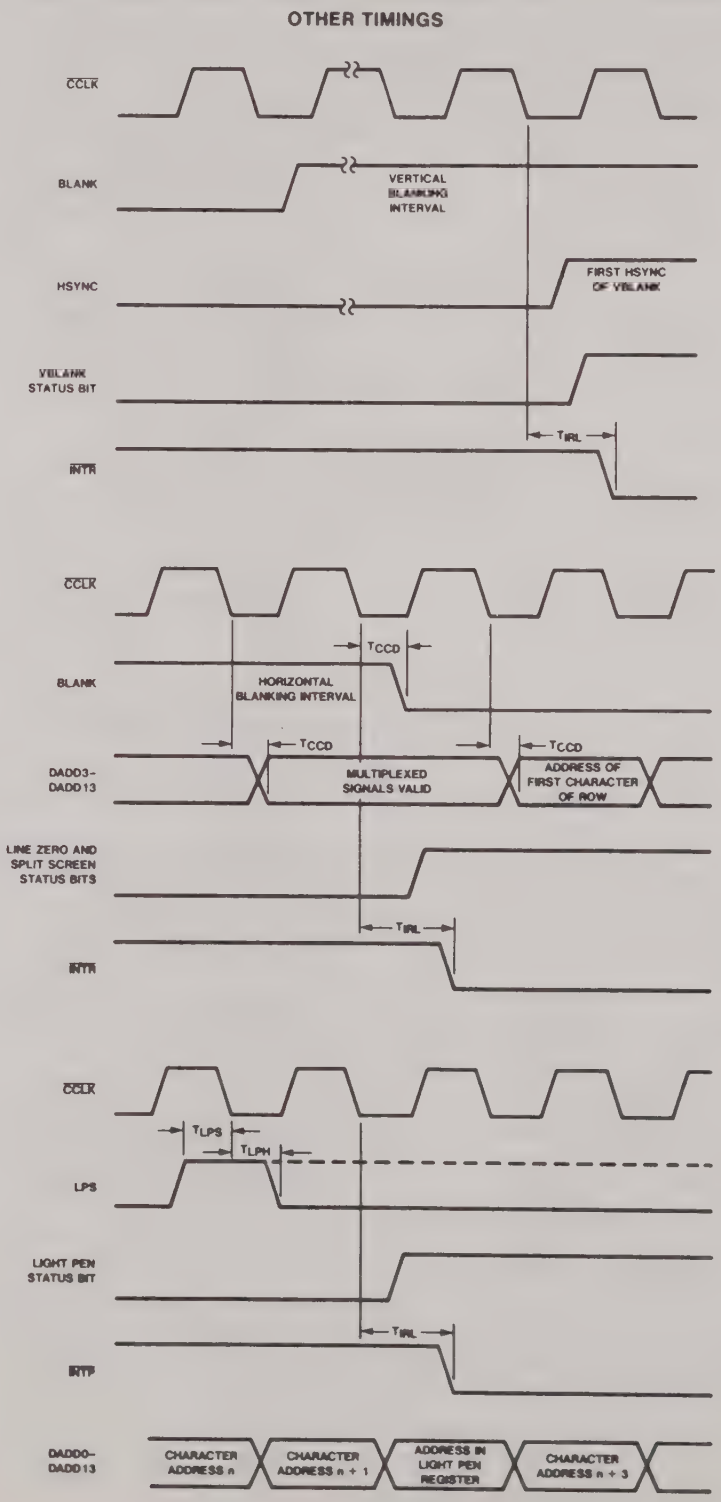

OTHER TIMINGS
CCLK
BLANK
VERTICAL BLANKING INTERVAL
HSYNC
FIRST HSYNC OF VBLANK
VBLANK STATUS BIT
TIRL
INTR
CCLK
TCCD
BLANK
HORIZONTAL BLANKING INTERVAL
TCCD
TCCD
DADD3-DADD13
MULTIPLEXED SIGNALS VALID
ADDRESS OF FIRST CHARACTER OF ROW
LINE ZERO AND SPLIT SCREEN STATUS BITS
TIRL
INTR
CCLK
TLPS
TLPH
LPS
LIGHT PEN STATUS BIT
TIRL
INTR
DADD0-DADD13
CHARACTER ADDRESS n
CHARACTER ADDRESS n + 1
ADDRESS IN LIGHT PEN REGISTER
CHARACTER ADDRESS n + 3

Figure 20

OTHER TIMINGS (Continued)

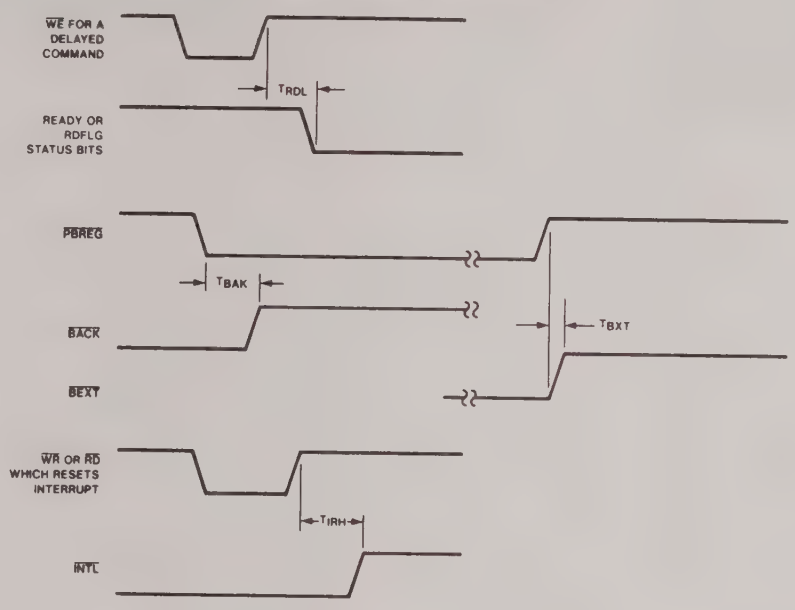
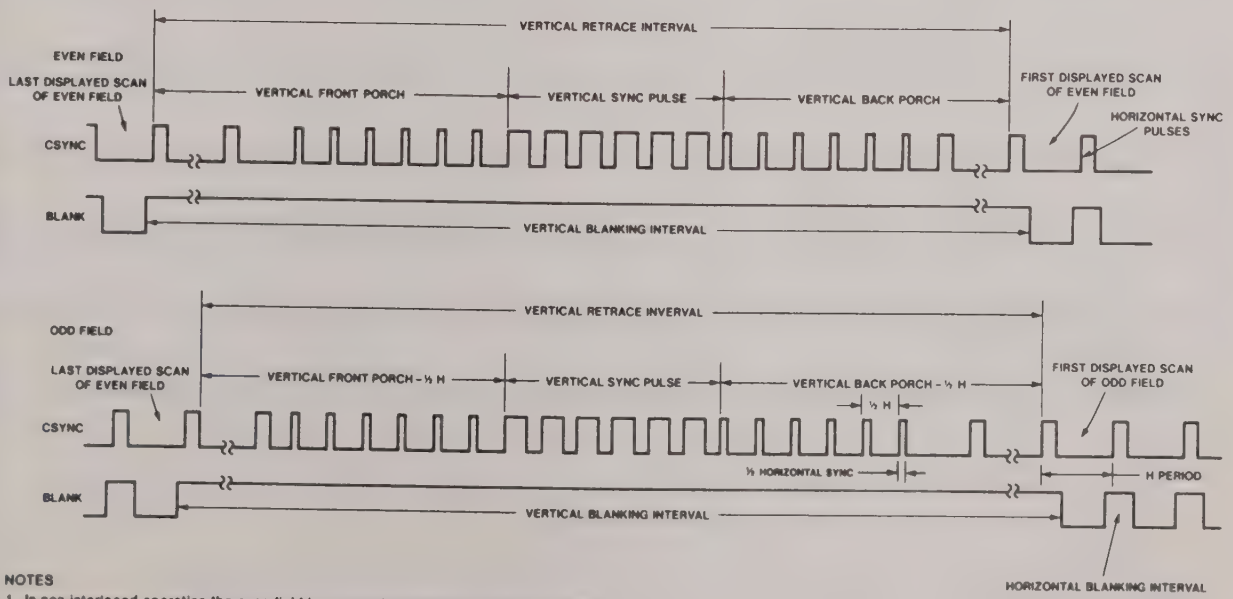


Figure 20

COMPOSITE SYNC TIMING



NOTES
1. In non-interlaced operation the even field is repeated continuously, and the odd field is not.
2. In interlaced operation the even field alternates with the odd field.

Figure 21

signetics

a subsidiary of U.S. Philips Corporation

Signetics Corporation
811 East Arques Avenue
P.O. Box 409
Sunnyvale, California 94086
Telephone 408/739-7700

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VIDEO ATTRIBUTES CONTROLLER (VAC) 2673

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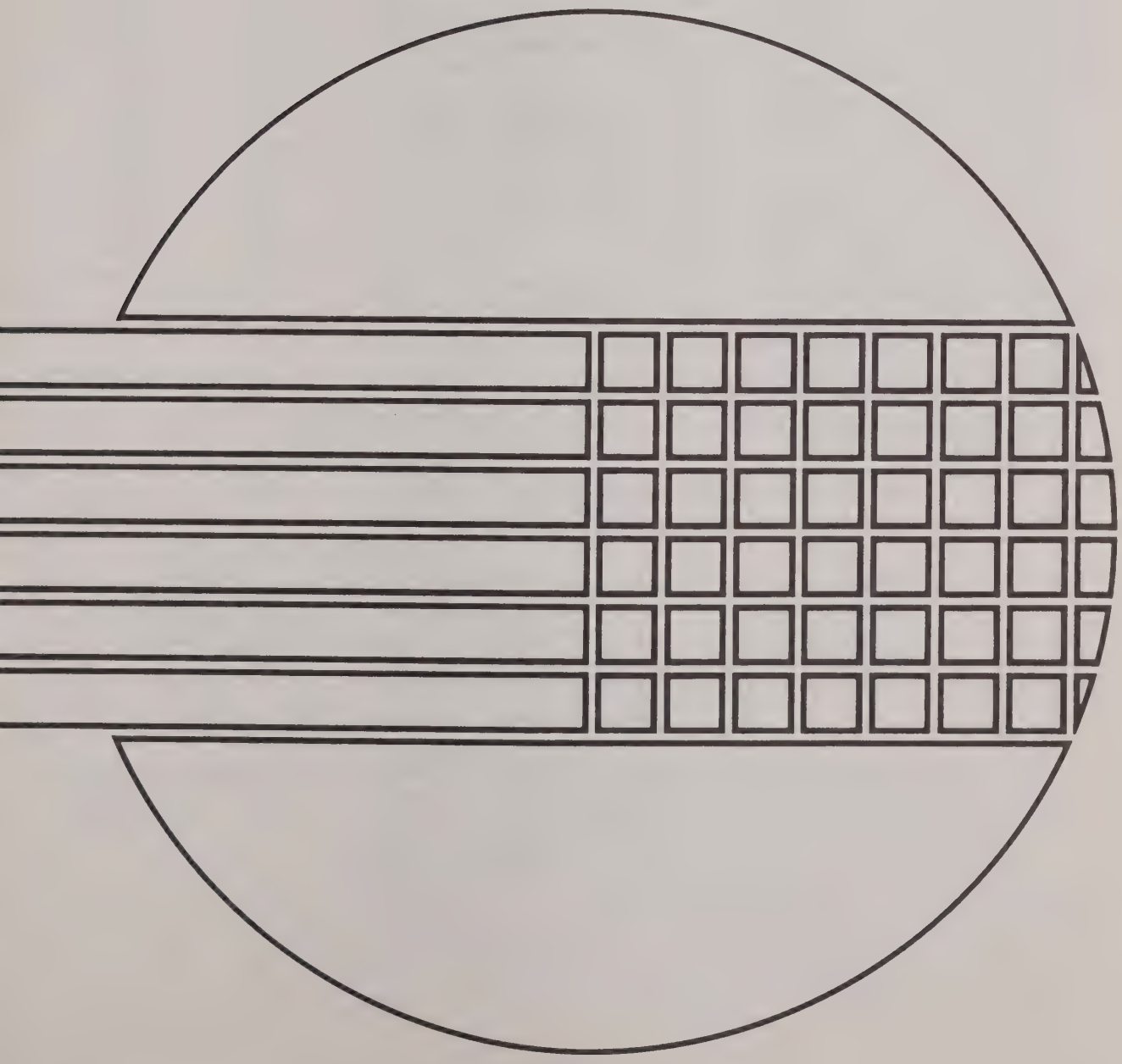


VIDEO ATTRIBUTES CONTROLLER (VAC) 2673/2673A

PRELIMINARY SPECIFICATION

DESCRIPTION

The Signetics 2673 and 2673A Video Attributes Controllers (VAC) are bipolar LSI devices designed for CRT terminals and display systems that employ raster scan techiques. Each contains a high speed video shift register, field and character attributes logic, attribute latch, cursor format logic and half dot shift control.

The VAC provides control of visual attributes on a field or character by character. Internal logic preserves field attribute data from character row to character row so that an attribute byte is not required at the beginning of each row. The 2673 provides for reverse video, blank (non-display), blink, underline and highlight attributes and a graphics mode attribute to work in conjunction with the Signetics 2670 Display Character and Graphics Generator (DCGG). The 2673A substitutes a light pen (strike-thru) attribute for the graphics attribute.

The horizontal dot frequency is the basic timing input to the VAC. Internally, this clock is divided down to provide a character clock output for system synchronization. Up to ten bits of video dot data are parallel loaded into the video shift register on each character boundary. The video data is shifted out on three outputs at the dot frequency. On the VIDEO output, the data is presented as a three level signal representing low, medium and high intensities. The three intensities are also encoded on two TTL compatible video outputs. Light or dark screen background can be selected.

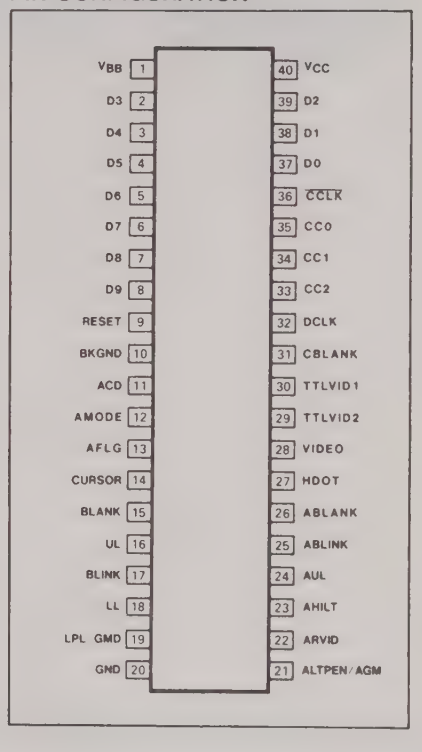
FEATURES

- **25MHz video dot rate**
- **Three level current driven (75 ohms) video output**
- **Three level encoded TTL video outputs**
- **Character/field attribute logic**
  - **Reverse video**
  - **Character blank**
  - **Character blink**
  - **Underline**
  - **Highlight**
  - **Light pen strike-thru or graphics control**
- **Field attributes extend from row to row**
- **Light or dark field**
- **Cursor reverse video logic**
- **Up to 10 dots per character**
- **Composite blanking for light field retrace**
- **Optional field graphics control output**
- **High speed bipolar design**
- **40 pin dual in-line package**
- **TTL compatible**
- **Compatible with Signetics 2672 PVTC and 2670 DCGG**

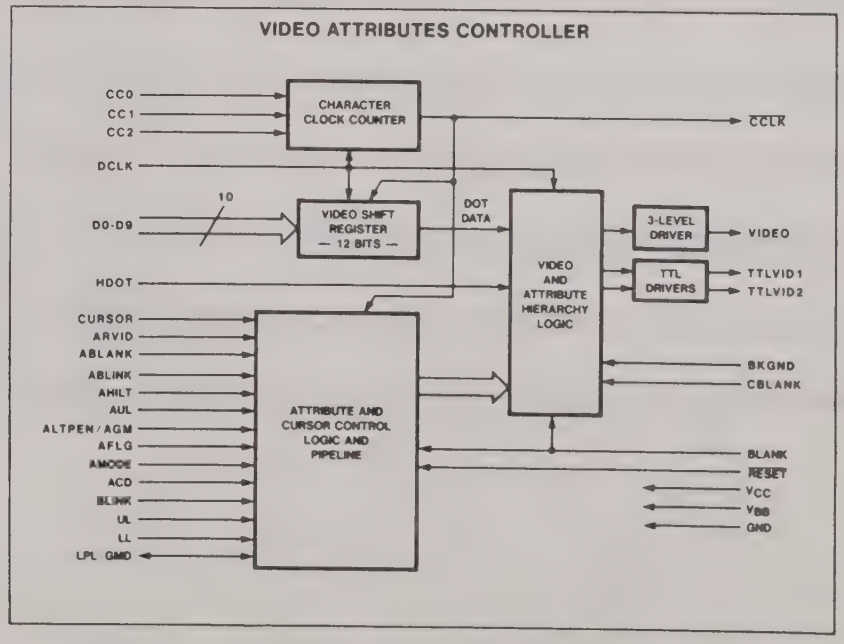
APPLICATIONS

- **CRT terminals**
- **Word processing systems**
- **Small business computers**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%, V_{BB} = 1.5V ± 10%, T_A = 0°C to 70°C	
	GRAPHICS ATTRIBUTE	LIGHT PEN ATTRIBUTE
Ceramic DIP	2673I	2673AI
Plastic DIP	2673N	2673AN

PIN DESIGNATION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
DCLK	32	I	**Dot Clock:** Dot frequency input. Video output shift rate.
$\overline{CCLK}$	36	O	**Character Clock:** A submultiple of DCLK. The frequency ranges from one sixth to one twelfth of DCLK, as determined by the state of the CC0-CC2 inputs.
CC2-CC0	33-35	I	**Character Clock Control:** The logic state on these three static inputs determine the internal divide factor for the $\overline{CCLK}$ output rate. Character clock rates of 6 thru 12 dots per character may be specified.
D0-D9	37-39, 2-8	I	**Dot Data Input:** These are parallel inputs corresponding to the character/graphic symbol dot data for a given scan line. These inputs are strobed into the video shift register on the falling edge of each character clock.
HDOT	27	I	**Half Dot Shift:** When this input is high, the serial video output is delayed by one half dot time. This input is latched on the falling edge of each character clock.
CURSOR	14	I	**Cursor Timing:** This input provides the timing for the cursor video. When high, effectively reverses the intensities of the video and attributes. Cursor position, shape, and blink rate are controlled by this input.
BKGND	10	I	**Background Intensity:** Specifies light or dark video during BLANK and character fields. Affects the intensities of all attributes.
BLANK	15	I	**Screen Blank:** When high, this input forces the video outputs to the level specified by the BKGND input (either high or low intensity). Not effective when CBLANK is high.
CBLANK	31	I	**Composite Blank:** When high, this input forces the video outputs to a low intensity state for retrace blanking. When BKGND input is low, this input may be tied low.
ARVID	22	I	**Reverse Video Attribute:** The intensity of the associated character or field video is reversed. All other attributes are effectively reversed.
AHILT	23	I	**Highlight Attribute:** All dot video (including underline) of the associated character or field is highlighted with respect to the BKGND input and the reverse video attribute.
ABLANK	26	I	**Blank Attribute:** Generates a blank space in the associated character or field. The blank space intensity is determined by the BKGND input, the reverse video attribute, and the CURSOR input.
ABLINK	25	I	**Blink Attribute:** The associated character or field video is driven to the intensity determined by BKGND and the reverse video attribute when the BLINK input is high.
AUL	24	I	**Underline Attribute:** Specifies a line to be displayed on the character or field. The line is specified by the UL input. All other attributes apply to the underline video.
ALTPEN/AGM	21	I	**Light Pen Attribute (2673A):** Specifies a highlighted line to be displayed on the character or field. The line is specified by the LPL input.
		I	**Attribute Graphics Mode (2673):** This input is latched and synchronized to provide a field GMD output for the 2670 DCGG.
AMODE	12	I	**Attribute Mode:** Specifies character (AMODE = 0) or field (AMODE = 1) attributes mode.
AFLG	13	I	**Attributes Flag:** The VAC samples and latches the attributes inputs when this input is high. If field attributes are specified (AMODE = 1), the attributes are double buffered on a row basis. Thus, each scan line of every character row will start with the attributes that were valid at the end of the previous row.
ACD	11	I	**Attribute Control Display:** In field attributes mode (AMODE = 1), if ACD = 0, the first character in each new attribute field (the attribute control character) will be suppressed and only the attributes will be displayed. If ACD = 1, the first character and the attributes are displayed. This input has no effect in character mode (AMODE = 0).
BLINK	17	I	**Blink:** This input is sampled on the falling edge of BLANK to provide the blink rate for the character blink attribute. It should be a submultiple of the frame rate.

PIN DESIGNATION (continued)

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
UL	16	I	**Underline:** Indicates the scan line(s) for the underline attribute. Latched on the falling edge of BLANK.
LPL/GMD	19	I	**Light Pen Line (2673A):** Indicates the scan line(s) for the light pen strike-thru attribute. Latched on the falling edge of BLANK.
		O	**Graphics Mode (2673):** This output provides a synchronized, latched, field graphics mode corresponding to the AGM input. This output can be used to control the GM input on the 2670 DCGG.
LL	18	I	**Last Line:** Indicates the last scan line of each character row. Used internally to extend field attributes across row boundaries. Latched on the falling edge of BLANK. This input has no effect in character mode (AMODE = 0).
VIDEO	28	O	**Video:** A three level serial video output which corresponds to the composite dot pattern of characters, attributes and cursor.
TTLVID1	30	O	**TTL Video 1:** This output corresponds to the serial, non-highlighted video dot pattern.
TTLVID2	29	O	**TTL Video 2:** This output corresponds to the highlighted serial video dot pattern. Should be used with TTLVID1 to decode a composite video of three intensities.
RESET	9	I	**Manual Reset:** This active high input initializes the internal logic and resets the attribute latches. Normally used for testing.
V_{CC}	40	I	**Power Supply:** +5 Volts ± 5%
V_{BB}	1	I	**Bias Supply:** +1.5 Volts ± 10%
GND	20	I	**Ground:** 0V reference

FUNCTIONAL DESCRIPTION

The VAC consists of four major sections (see block diagram). The high speed dot clock input is divided internally to provide a character clock for system timing. The parallel dot data is loaded into the video shift register on each character boundary and shifted into the video logic block at the dot rate. The six attribute inputs are latched internally and combined with the serial dot data to provide a three level video source for the monitor.

A separate BLANK input defines the active screen area. When BLANK = 0, the video levels are derived internally by the combinations of dot data, attributes, cursor, and the state of the BKGND input. Either black or white background can be selected. Symbols (dot data) are normally gray and can be highlighted to white or black as shown in figure 1.

During the inactive screen area (BLANK = 1), the video level is either white (BKGND = 1) or black (BKGND = 0). A separate composite blank input (CBLANK) is provided to suppress the border video during CRT retrace when white background is specified.

Character Clock Counter

The character clock counter divides the frequency on the DCLK input to generate the character clock ($\overline{CCLK}$). The divide factor is specified by the clock control inputs (CC0-CC2) as follows:

			$\overline{CCLK}$	
CC2	CC1	CC0	DOTS/CHARACTER	DUTY CYCLE
0	0	0	6	3/3
0	0	1	6	3/3
0	1	0	7	4/3
0	1	1	8	4/4
1	0	0	9	5/4
1	0	1	10	5/5
1	1	0	11	6/5
1	1	1	12	6/6

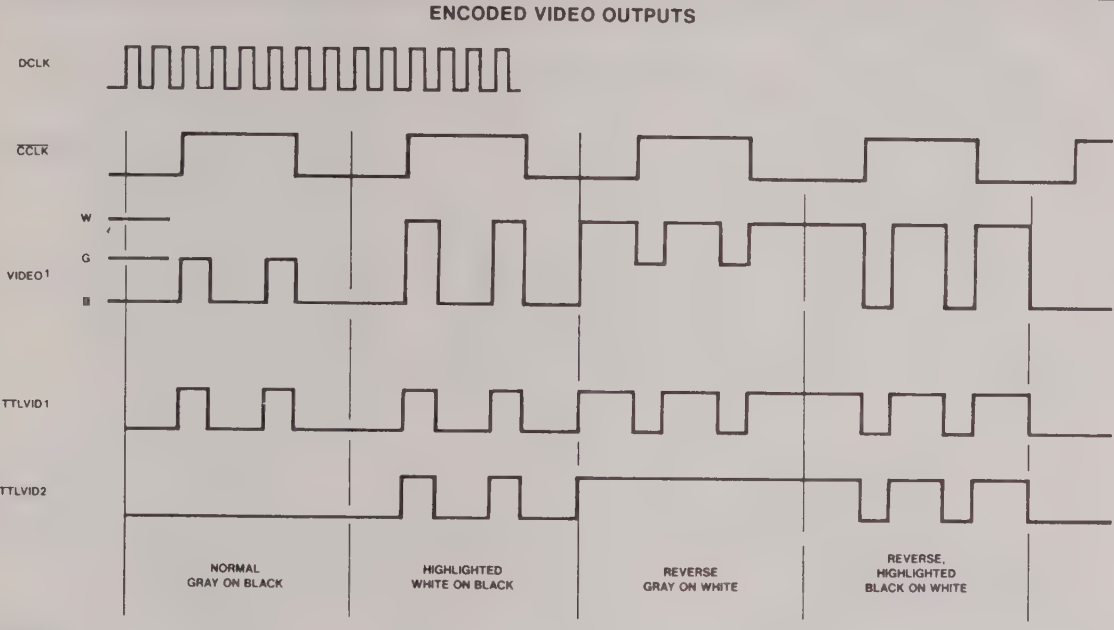
Video Shift Register

On each character boundary, the parallel data (D0-D9) is loaded into the video shift register. The data is shifted out least significant bit first (D0) by the DCLK. If 11 or 12 dots/character are specified (CC2-CC0 = 110 or 111), a 0 (blank dot) is always shifted out before D0. For 12 dots/character, a 0 is also shifted out after D9. The serial dot data is shifted into the video logic where it is combined with the cursor and attributes to encode three levels of video.

Attribute and Cursor Control

The VAC visual attributes capabilities include: reverse video, character blank, blink, underline, highlight, and light pen strike-thru. The six attributes and the three attribute control inputs (AMODE, AFLG, and ACD) are clocked into the VAC on the falling edge of $\overline{CCLK}$. If AFLG is high, the attributes are latched internally and are effective for either one character time (AMODE = 0) or until another set of attributes is latched (AMODE = 1). The attributes set is double buffered on a row by row basis internally. Using this technique, field attributes can extend across character row boundaries thereby eliminating the necessity of starting each row with an attribute set.

When field attribute mode is selected, (AMODE = 1), the VAC will accommodate two attribute storage configurations. In one configuration, the attribute control data is stored in the refresh RAM, taking the place of the first character code in the field to be affected. For this mode, the ACD input is tied low and blank characters will be displayed in the screen positions occupied by the attribute data (see figure 10). In the second configuration, (ACD = 1), the character codes and attribute data are presented to the VAC in parallel. In this mode, dot data is displayed at each character position (see figure 11).



NOTE
1. W = White
G = Gray
B = Black

Figure 1

The CURSOR and the attribute input signals are pipelined internally to allow for system propagations (one $\overline{CCLK}$ for refresh RAM, one $\overline{CCLK}$ for dot generator). The attribute timing signals BLINK, UL, LPL and LL are clocked into the VAC at the beginning of each scan line by the falling edge of the BLANK input. Thus, these signals must be in their proper state at the falling edge of BLANK preceding the scan line at which they are to be active (see figure 4).

Video Logic

The serial dot data and the pipelined cursor and attributes are combined to generate the three level current source on the VIDEO output. The three levels (white, gray, and black) are also encoded on the two TTL compatible outputs TTLVID1 and TTLVID2. The three levels are encoded as shown.

The video is normally shifted out on the leading edge of the DCLK. When the HDOT input is asserted, the corresponding dot data is delayed by one-half DCLK. This half dot shifting, when used on selected lines of character video, can be used to effect eye-pleasing character rounding as shown in figure 2.

TTLVID2	TTLVID1	INTENSITY
0	0	Black (or CBLANK)
0	1	Gray (on black surround)
1	0	Gray (on white surround)
1	1	White

NOTE
The TTLVID1 output can be used independently to generate a two level non-highlighted video.

Attribute Hierarchy

The video of each character block consists of four components as shown in figure 3.

Symbol video is generated from the dot data inputs D0-D9.

Underline video is enabled by the AUL attribute and is generated when the UL timing input is active. Underline and symbol video are always the same intensity.

Strike-thru video is enabled by the ALTPEN attribute and is generated when the LPL timing input is active. This video is always highlighted and takes precedence over the symbol and underline video. This feature applies to the 2673A only.

Surround video is the absence of symbol, underline and strike-thru video or the presence of the non-display attributes (ABLANK or ABLINK • BLINK).

The relative intensities of the four video components are determined by the remaining attributes (AHILT, ABLANK, ABLINK, ARVID) and the BKGND and CURSOR inputs as illustrated in table 1.

"AT" SYMBOL WITH AND WITHOUT HALF DOT SHIFTING

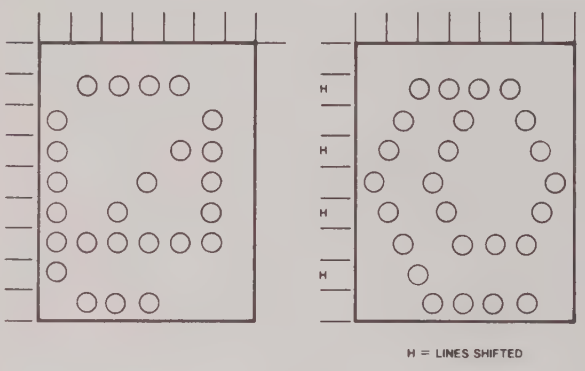


Figure 2

VIDEO COMPONENTS OF CHARACTER BLOCK

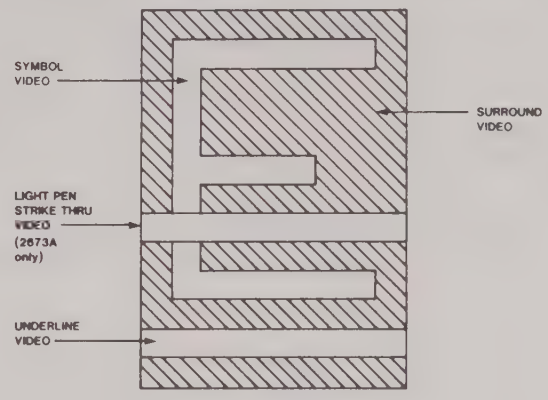


Figure 3

ATTRIBUTES AND CONTROL INPUTS d = don't care				RELATIVE VIDEO INTENSITIES W = White, B = Black, G = Gray		
BKGND	REVERSE[1]	NON-DISPLAY[2]	AHILT	STRIKE THRU VIDEO[3]	SYMBOL OR UNDERLINE VIDEO[3,4]	SURROUND VIDEO[3]
0	0	0	0	W	G	B
0	0	0	1	W	W	B
0	0	1	d	B	B	B
0	1	0	0	B	G	W
0	1	0	1	B	B	W
0	1	1	d	W	W	W
1	0	0	0	B	G	W
1	0	0	1	B	B	W
1	0	1	d	W	W	W
1	1	0	0	W	G	B
1	1	0	1	W	W	B
1	1	1	d	B	B	B

NOTES
1. Reverse = ARVID • $\overline{\text{CURSOR}}$ + $\overline{\text{ARVID}}$ • CURSOR
2. Non-display = ABLANK + ABLINK • BLINK
3. See figure 3
4. Symbol and underline video are always the same intensity.

Table 1. ATTRIBUTES HIERARCHY

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
Operating ambient temperature[2]	0 to +70	°C
Storage temperature	−65 to +150	°C
All voltages with respect to ground	−0.5 to +6.0	V

NOTES
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature and thermal resistance of 60°C/W junction to ambient (ceramic package).

DC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = +1.5V \pm 10\%$[3,4,5]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage		2.0			V
V_{OL}	Output low voltage (except VIDEO)	$I_{OL} = 1.6mA$			0.4	V
V_{OH}	Output high voltage (except VIDEO)	$I_{OH} = -100\mu A$	2.4			V
V_B	VIDEO black level	$R_L = 75\Omega$ to GND		0		V
V_G	VIDEO gray level	$R_L = 75\Omega$ to GND		0.225		V
V_W	VIDEO white level	$R_L = 75\Omega$ to GND		0.50		V
I_{IL}	Input low current	$V_{IN} = 0.4V$			−400/ −800[10]	μA
I_{IH}	Input high current	$V_{IN} = 2.4V$			20/40[10]	μA
I_{CC}	V_{CC} supply current	$V_{IN} = 0V$, V_{CC} = max			50	mA
I_{BB}	V_{BB} supply current	V_{BB} = max			100	mA

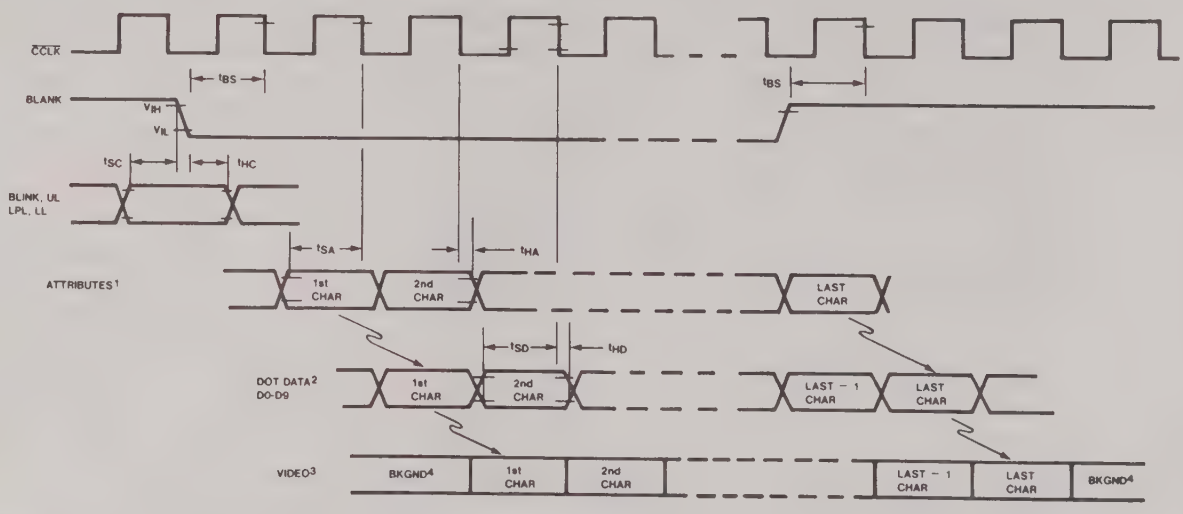
AC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = +1.5V \pm 10\%$[3,4,5]

PARAMETER		TEST CONDITIONS	TENTATIVE LIMITS			UNIT
			Min	Typ	Max	
Dot clock[6]						
f_D	frequency				25	MHz
t_{DH}	high		15			ns
t_{DL}	low		15			ns
Setup times to $\overline{CCLK}$[7]						
t_{BS}	BLANK		35			ns
t_{SC}	BLINK, UL, LPL, LL (ref to BLANK)		20			ns
t_{SA}	Attributes		35			ns
t_{SD}	Dot data D0-D9		70			ns
t_{SK}	CURSOR		35			ns
t_{FS}	AFLG		50			ns
t_{SH}	HDOT		35			ns
Hold times from $\overline{CCLK}$[7]						
t_{HC}	BLINK, UL, LPL, LL (ref to BLANK)		20			ns
t_{HA}	Attributes		35			ns
t_{HD}	Dot data D0-D9		0			ns
t_{HK}	CURSOR		35			ns
t_{FH}	AFLG		50			ns
t_{HH}	HDOT		35			ns
Setup times to DCLK[8]						
t_{SG}	BKGND		15			ns
t_{SB}	CBLANK		15			ns
Hold times from DCLK[8]						
t_{HG}	BKGND		15			ns
t_{HB}	CBLANK		15			ns
Delay times[9]		$C_L = 150pF$				
t_{DGM}	GMD from DCLK				60	ns
t_{DC}	CCLK from DCLK				60	ns
t_{DV}	VIDEO, TTLVID1, and TTLVID2 from DCLK				75	ns

NOTES

3. Parameters are valid over operating temperature range unless otherwise specified.
4. All voltage measurements are referenced to ground (V_{SS}). All input signals swing between 0.4V and 2.4V. All time measurements are referenced at input voltages of 0.8V, 2.0V and at output voltages of 0.8V, 2.0V as appropriate.
5. Typical values are at +25°C, typical supply voltages and typical processing parameters.
6. See figure 7
7. See figures 4, 5, 6, and 9
8. See figure 8.
9. See figures 6 and 7.
10. For DCLK input

VAC PIPELINE TIMING



NOTES
1. Attributes include: ABLINK, ABLANK, ARVID, AUL, AHILT, and ALTPEN.
2. One $\overline{CCLK}$ delay for dot data (obtained from delay through character generator).
3. See figure 7 for detail timing of VIDEO, TTLVID1, TTLVID2.
4. Non-active scan time. VIDEO reverts to polarity selected by the BKGND input.

Figure 4

CURSOR PIPELINE TIMING

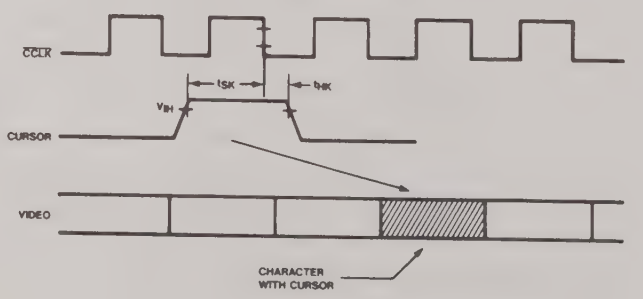
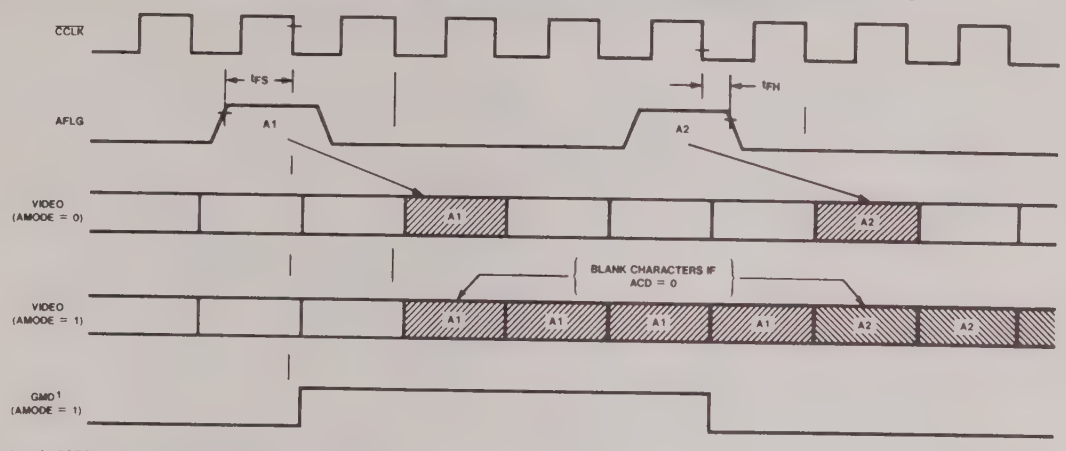


Figure 5

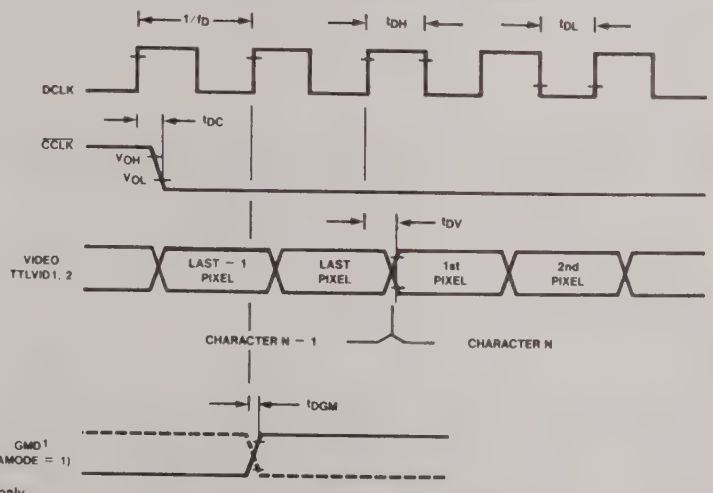
CHARACTER (AMODE = 0), FIELD (AMODE = 1), AND GMD ATTRIBUTE TIMING



NOTE
1. GMD output in 2673 version only. See figure 7 for detail timing.

Figure 6

VIDEO AND GMD PIPELINE TIMING



NOTE
1. GMD output in 2673 version only.

Figure 7

BKGND AND CBLANK TIMING DURING INACTIVE SCAN TIME (BLANK = 1)

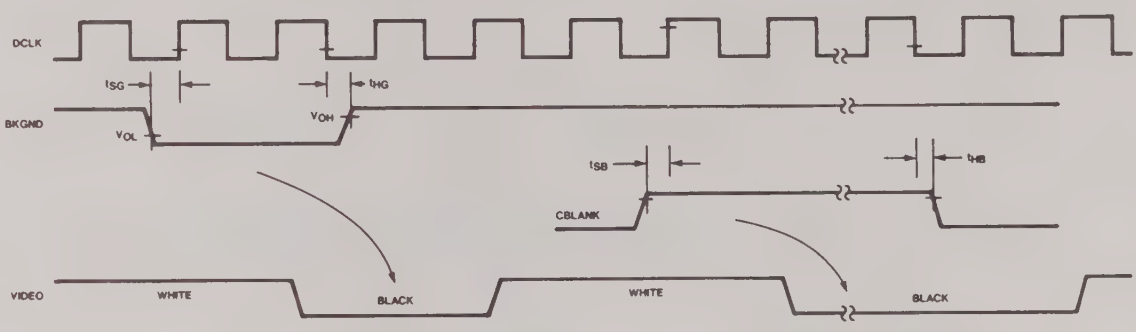


Figure 8

HALF DOT SHIFT TIMING

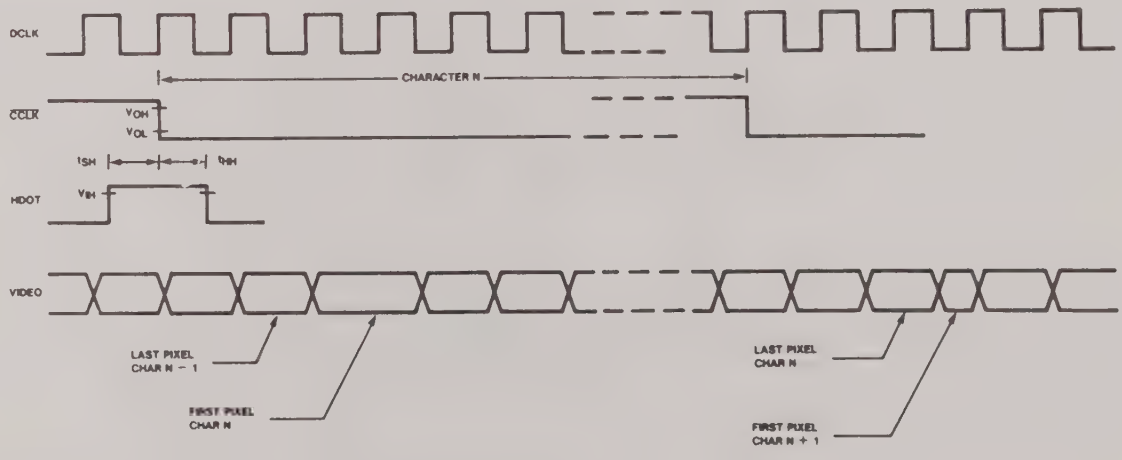


Figure 9

SYSTEM BLOCK DIAGRAM OF THE 2673 IN FIELD ATTRIBUTE MODE USING THE NARROW RAM (8 WIDE) CONFIGURATION

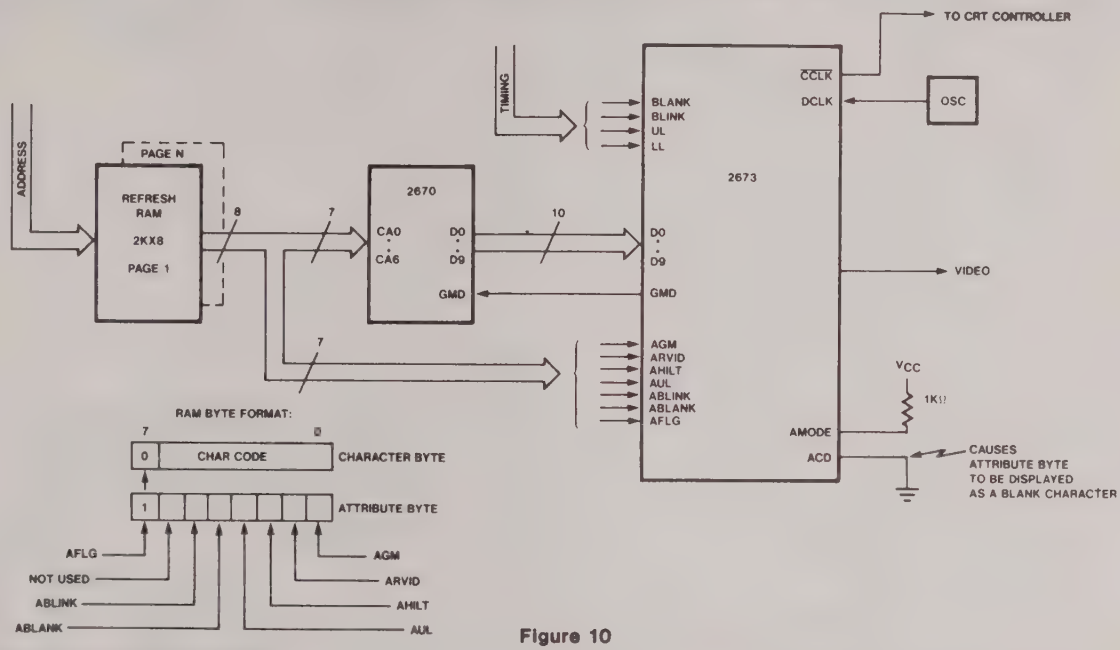
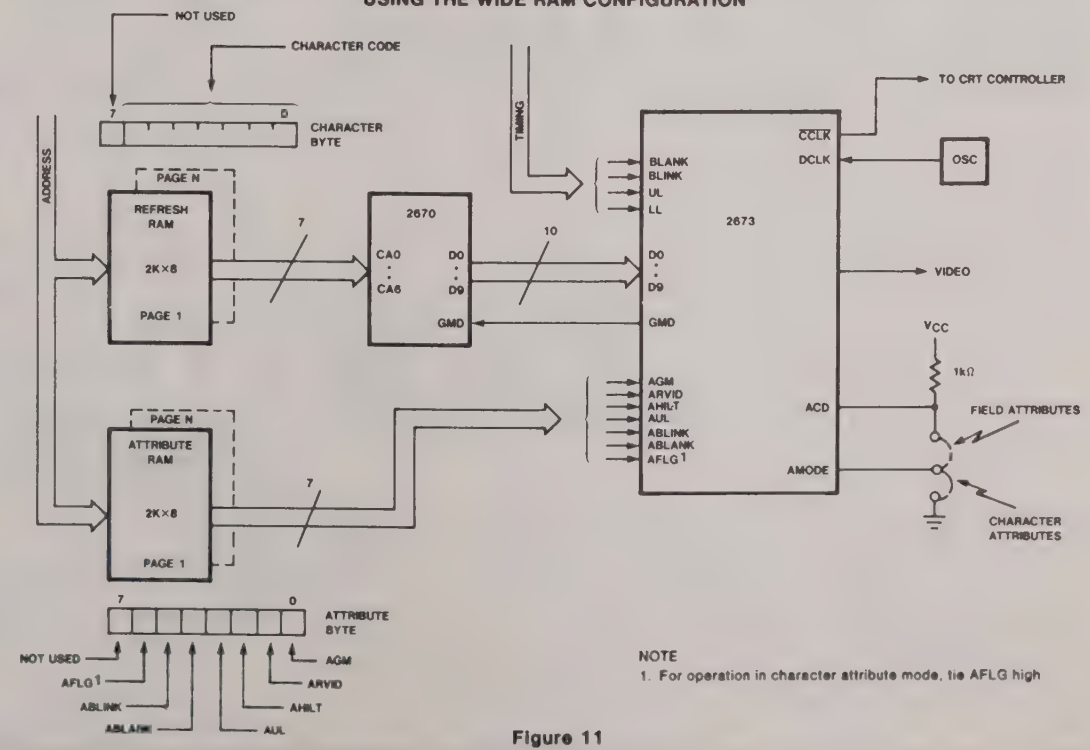


Figure 10

SYSTEM BLOCK DIAGRAM OF THE 2673 IN FIELD OR CHARACTER ATTRIBUTE MODE USING THE WIDE RAM CONFIGURATION



NOTE
1. For operation in character attribute mode, tie AFLG high

Figure 11

VIDEO OUTPUT STAGES OF THE 2673

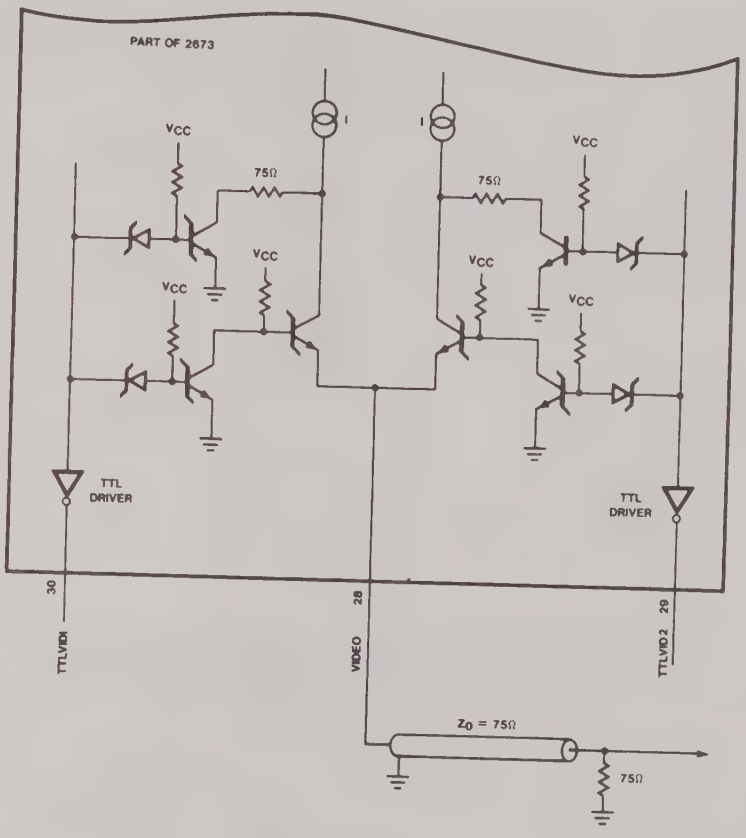


Figure 12

signetics
a subsidiary of U.S. Philips Corporation
Signetics Corporation
811 East Arques Avenue
P.O. Box 409
Sunnyvale, California 94086
Telephone 408/739-7700

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April 1981

Using The 2670/71/72/73 CRT Terminal Chip Set

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USING THE 2670/71/72/73 CRT TERMINAL CHIP SET App Note 401

INTRODUCTION

Microprocessors and LSI have had a dramatic impact on the implementation and capabilities of alphanumeric CRT terminals. The first generation of CRT terminals were little more than 'glass teletypes'. Current designs, implemented with microprocessors, are characterized by an abundance of sophisticated features that were previously not economically feasible: a universal hardware design that can adapt to different user requirements simply by changing software or firmware; programmability to provide end users with the flexibility to execute specialized routines; and local intelligence and storage which off-loads the host CPU by permitting data manipulation and verification at the terminal site.

Just as the impact of microcomputers has been felt in the functional capabilities of terminals, advances in semiconductor technology have revolutionized the hardware implementation. Designs that previously consisted of 100 to 200 ICs can now be realized with a few dozen MSI and LSI devices. The majority of the LSI manufacturers' effort with respect to CRT terminals has been concentrated in the 'CRT controller' area. These circuits provide the character timing, display addressing, and sync generation functions required by all terminals. However, these controllers need to be supported by many other external circuits to implement a complete terminal.

The purpose of this application note is to provide information on the use of four new Signetics CRT terminal products which, when combined with standard CPUs, memories, and TTL, allow the implementation of a wide spectrum of CRT terminal capabilities in as few as 15 total packages. These devices are:

- 2670 Display Character and Graphics Generator (DCGG)
- 2671 Programmable Keyboard and Communications Controller (PKCC)
- 2672 Programmable Video Timing Controller (PVTC)
- 2673 Video and Attributes Controller (VAC)

MAJOR ELEMENTS OF A CRT TERMINAL

Figure 1 shows the major elements of a typical low-end microcomputer-based CRT terminal. In this system, the CPU examines inputs from the data communications line and the keyboard and places the data to be displayed in a display buffer memory, which is typically a RAM which holds the data for a single or multiple screenload (page) or for a single character row. High-end ('smart' and 'intelligent') terminals start with the same base, but append additional circuits to provide more features and capabilities. The following sections describe the functions of each of the major blocks.

Character Timing and Sync Generation

The major function of this block is to generate the horizontal and vertical timing signals required to produce the TV raster on the CRT monitor. Other functions include the generation of display memory addresses in synchronism with the monitor scan and in accordance with a defined screen format (characters per row, scan lines per row and rows per screen), generation of a cursor signal at the appropriate scan position, and generation of video blanking signals during retrace intervals.

CRT TERMINAL BLOCK DIAGRAM

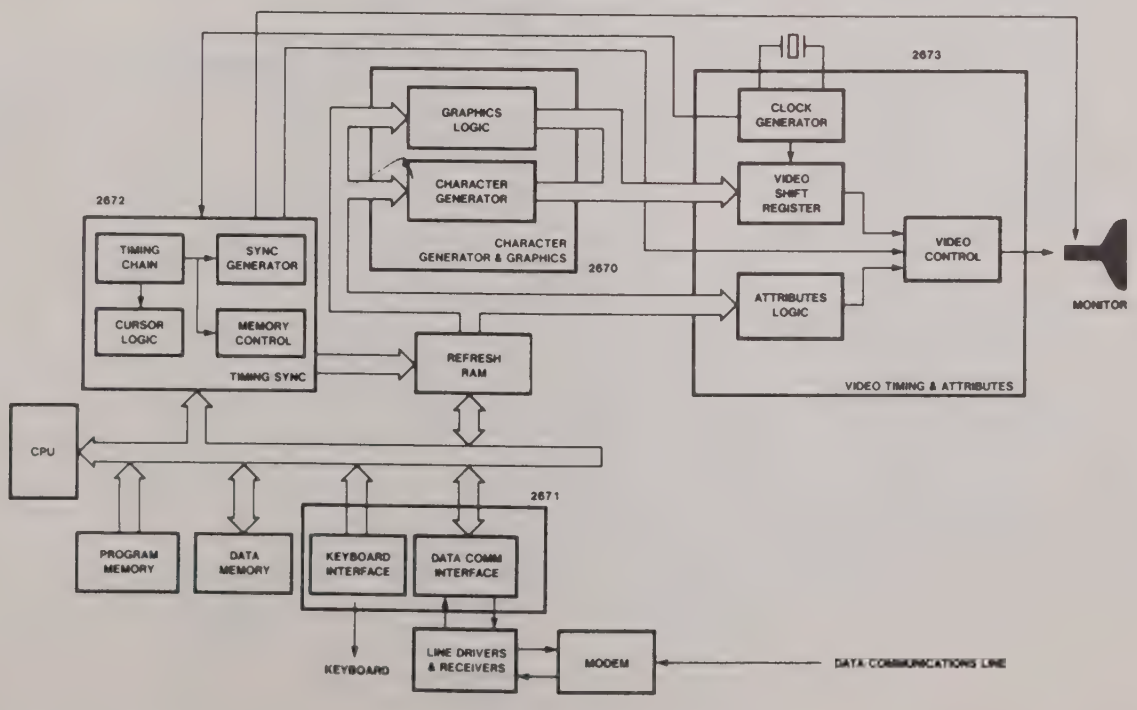

Figure 1

I/O Interface

In its simplest form, this block provides an interface to a keyboard to identify the key depressed and a serial communications link, normally operating in an asynchronous format, between the terminal and the host computer. Although these functions could be performed programmatically by the terminal CPU system, removing these functions to intelligent controllers unburden the system CPU and allow it to be used more effectively to provide additional features with a relatively small cost impact.

Character and Graphics Generation

These circuits convert the data stored in the display memory to the line by line dot patterns required to display the data on the CRT monitor.

Video Timing and Visual Attributes

This section contains the high speed (dot rate) circuits necessary to convert the parallel data from the character and graphics generation circuits to the serial video stream required by the CRT. Also included are circuits to sum visual display attributes such as blinking, high/low intensity, reverse video, and underlining into the video stream.

SIGNETICS' CRT CHIP SET

As mentioned previously, the Signetics CRT 'set' consists of four circuits. The functions of these circuits correspond closely to the four major CRT terminal blocks described above. The circuits have been partitioned so as to allow each to be used independent of the others, allow several alternative methods of implementing the display memory interface so that the hardware can be tailored to the system requirements, provide a full complement of programmable capabilities, and minimize the number of support circuits required.

The following sections give a brief description of each of the circuits. The reader is referred to the individual data sheets for full operational details.

2672 Programmable Video Timing Controller (PVTC)

The 2672 PVTC, figure 2, is a programmable device designed for use in CRT terminals and display systems that employ raster scan techniques. The PVTC generates the vertical and horizontal timing signals necessary for the display of interlaced or non-interlaced data on a CRT monitor. Also, the 2672 provides consecutive addressing to a user specified display buffer memory domain and controls the CPU-display buffer interface for various buffer configuration modes. A variety of operating modes, display formats, and timing profiles can be implemented by programming the control registers in the PVTC.

The CPU initializes the 2672 control and timing registers for the desired timing profiles and memory configuration. The PVTC provides the handshake control for CPU access to the display buffer. One of four memory access modes may be programmed: independent mode, trans-

2672 PROGRAMMABLE VIDEO TIMING CONTROLLER

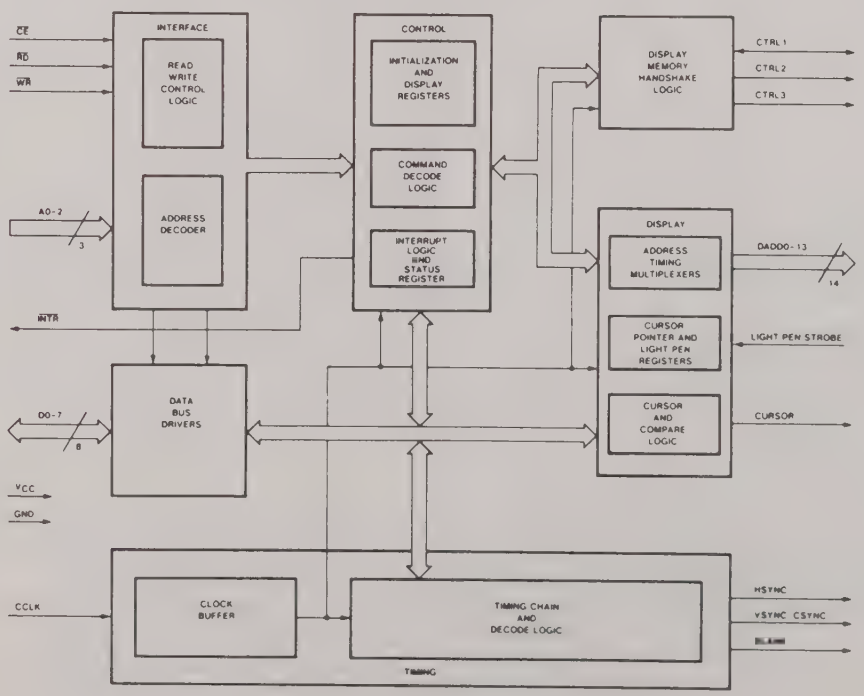

Figure 2

parent mode, shared mode, and row mode. These modes are described in the System Configurations section of this application note.

In all modes, the PVTC provides addresses for the display buffer which outputs the character codes to the 2670 Display Character and Graphics Generator (DCGG) and visual attribute codes to the 2673 Video Attributes Controller (VAC). The DCGG and PVTC supply the dot data and sync timing to the VAC which generates the serialized video.

Programmable features of the PVTC include screen format (characters/row, rows/screen, scan lines/row), horizontal and vertical timing parameters, cursor type (block or underline) and blink rate, character blink rate, interlaced or non-interlaced operation, and single or double height characters.

The PVTC is capable of producing interrupts based upon several internal conditions. By using these interrupts (or by polling the equivalent status register) display features such as non-consecutive buffer addressing for split screen operation, multiple cursors, horizontal and vertical scrolling, and smooth vertical scroll can be implemented

2671 Programmable Keyboard and Communications Controller (PKCC)

The 2671, figure 3, is an MOS LSI device which provides a versatile keyboard interface and also functions as an asynchronous communications controller. It is intended for use in microprocessor based systems and provides an eight bit data bus interface.

The keyboard controller handles the scanning, debounce, and encoding of mechanical or capacitive keyboards with a maximum of 128 keys utilizing any of four programmable rollover modes. A mask programmable ROM provides four levels of key encoding, corresponding to the separate shift and control input combinations. An eight bit keyboard status register transmits status information to the CPU. Programmable features include rollover mode, scan rate and debounce time, coded or uncoded operation, and automatic repeat operation.

The communications section of the PKCC is a universal asynchronous receiver and transmitter (UART). The receiver accepts serial input data and converts it to parallel data characters. Simultaneously, the transmitter accepts parallel data from the CPU data bus and outputs it in serialized form. Received data is checked for parity and framing errors, and break conditions are flagged. Character lengths can be programmed as 5, 6, 7, or 8 bits not including parity, start or stop bits. An internal baud rate generator (BRG) operating from an external clock or directly from a crystal can be used to derive one of sixteen receive and/or transmit clocks. An eight bit communications status register provides status information to the CPU.

The PKCC has an interrupt mask register to selectively enable keyboard and communications status bits to generate interrupts. Priority encoded interrupt vectoring is available. Upon receipt of an interrupt acknowledge, a mask programmable interrupt vector will be output on the data bus reflecting the source of the interrupt. The mask enabled interrupt sources can also be read directly.

2670 Display Character and Graphics Generator (DCGG)

The DCGG, figure 4, is a mask-programmable 11,648-bit line select character generator. It contains 128 10x9 characters placed in a 10x16 matrix, and has the capability of shifting certain characters, such as j, y, g, p and q, that normally extend below the baseline; effectively, the 9 active lines are lowered within the matrix to compensate for the character's position.

Seven bits of an 8-bit address code are used to select 1 of the 128 available characters. The eighth bit functions as a chip enable signal. Each character is defined by a pattern of logic 1s and 0s stored in a 10x9 matrix. When a specific 4-bit binary line address code is applied, a word of 10 parallel bits appears to the output. The lines can be sequentially selected, providing a 9-word sequence of 10 parallel bits per word for each character selected by the address inputs. As the line address inputs are sequentially addressed, the device will automatically place the 10x9 character in 1 of 2 preprogrammed positions on the 16-line matrix with the positions defined by the 4-line address inputs. One or more of the 10 parallel outputs can be used as control signals to selectively enable functions such as half-dot shift, color selection, etc.

The 2670 DCGG includes latches to store the character address and line address data. A control input to inhibit character data output for certain groups of characters is also provided. The 2670 also includes a graphics capability, wherein the 8-bit character code is translated directly into 256 possible user programmable graphic patterns. Thus, the DCGG can generate data for 384 distinct patterns, of which 128 are defined by the mask programmable ROM.

2673 Video and Attributes Controller (VAC)

The 2673, figure 5, is a bipolar LSI device designed for CRT terminals and display systems that employ raster scan techniques. It contains a high speed video shift register, field and character attributes logic, attribute latch, cursor format logic and half dot shift control, and can be programmed for a light or dark screen background.

The VAC visual attribute capabilities are reverse video, character blank, blink, underline, highlight, and light pen strike-thru or, optionally, graphics. Each attribute has a separate control input which is latched internally when the AFLAG input is asserted. If the AMODE input is low, the attributes are valid for one character time. If AMODE is high, the attributes remain valid until the field is terminated by strobing in a new attributes set. The attributes are double buffered on a row by row basis internally so that field attributes can extend across character row boundaries thereby eliminating the necessity of starting each row with an attribute set.

The horizontal dot frequency is the basic timing input element to the VAC; internally, this clock is divided down to provide a character clock output for system synchronization. Ten bits of dot data are parallel loaded into the video shift register on each character boundary. The video data is shifted out on three outputs at the dot frequency. On the video output, the video is presented as a three level signal representing low, medium and high intensities, and the three intensities are also encoded on the two TTL compatible video outputs.

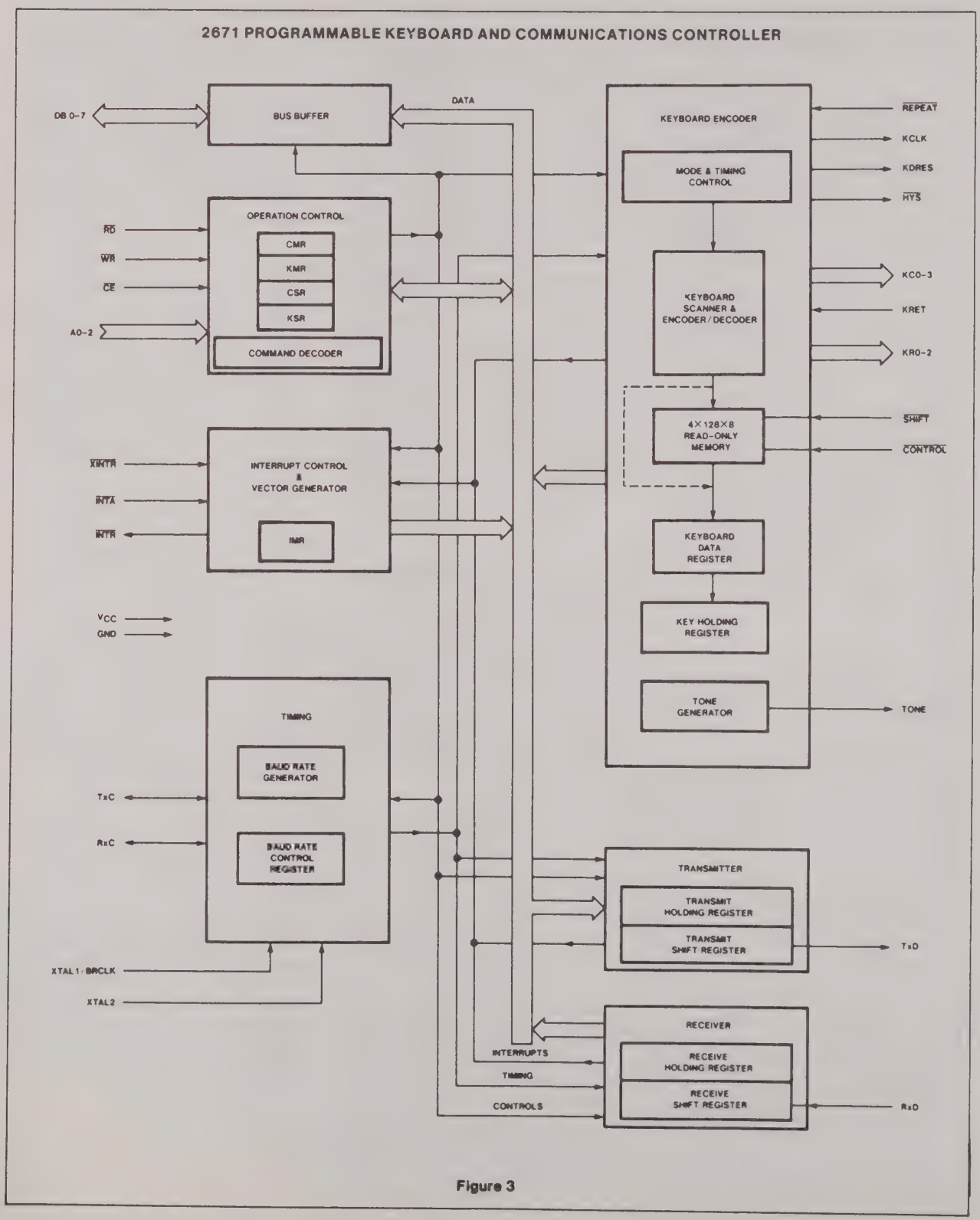
2671 PROGRAMMABLE KEYBOARD AND COMMUNICATIONS CONTROLLER
DB 0-7
BUS BUFFER
DATA
KEYBOARD ENCODER
REPEAT
KCLK
MODE & TIMING CONTROL
KDRES
HYS
OPERATION CONTROL
CMR
KMR
CSR
KSR
COMMAND DECODER
RD
WR
CE
A0-2
KEYBOARD SCANNER & ENCODER/DECODER
KC0-3
KRET
KR0-2
4X128X8 READ-ONLY MEMORY
SHIFT
CONTROL
XINTR
INTA
INTR
INTERRUPT CONTROL & VECTOR GENERATOR
IMR
KEYBOARD DATA REGISTER
KEY HOLDING REGISTER
VCC
GND
TONE GENERATOR
TONE
TIMING
BAUD RATE GENERATOR
BAUD RATE CONTROL REGISTER
TxC
RxC
XTAL1/BRCLK
XTAL2
TRANSMITTER
TRANSMIT HOLDING REGISTER
TRANSMIT SHIFT REGISTER
TxD
RECEIVER
RECEIVE HOLDING REGISTER
RECEIVE SHIFT REGISTER
RxD
INTERRUPTS
TIMING
CONTROLS

Figure 3

2670 DISPLAY CHARACTER AND GRAPHICS GENERATOR

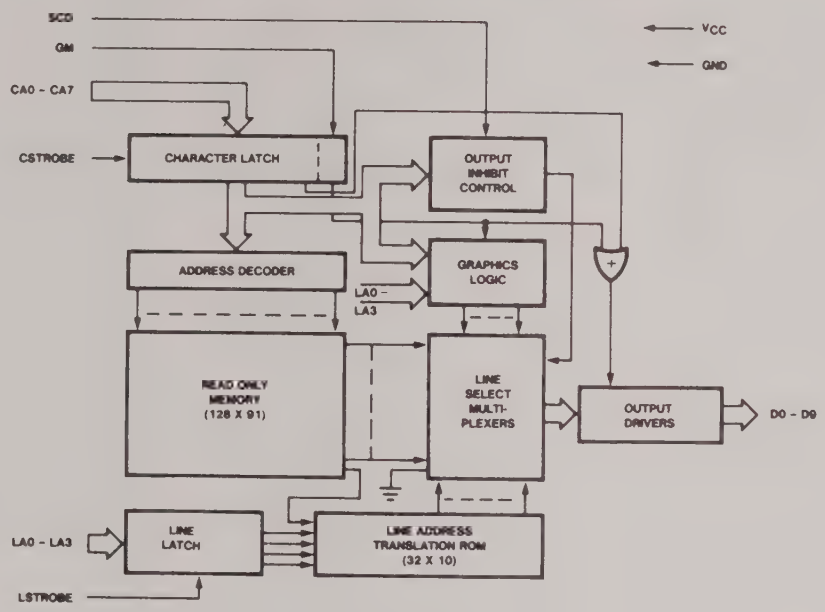

Figure 4

2673 VIDEO AND ATTRIBUTES CONTROLLER

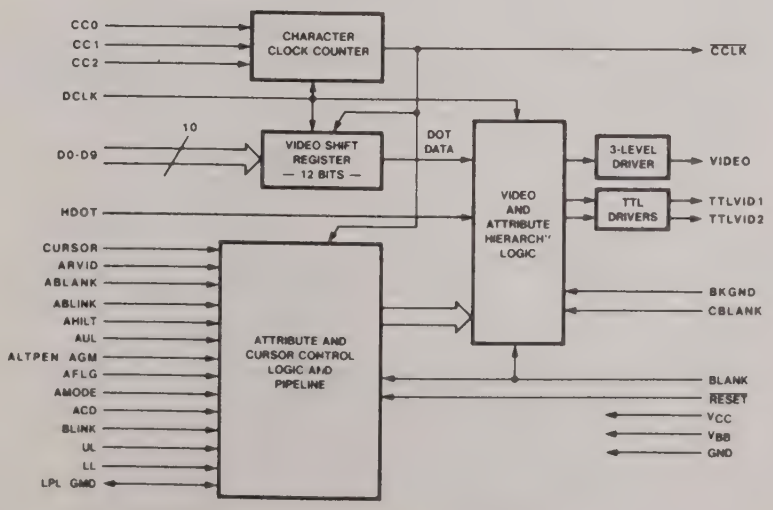

Figure 5

SYSTEM CONFIGURATIONS

The PVTC supports four common system configurations of display buffer memory interface, designated the independent, transparent, shared, and row buffer modes. The first three modes utilize a single or multiple page RAM and differ primarily in the means used to transfer display data between the RAM and the CPU. The row buffer mode makes use of a single row buffer (which can be a shift register or a small RAM) that is updated in real time to contain the appropriate display data.

Independent Mode

The CPU to RAM interface configuration for this mode is illustrated in figure 6. Transfer of data between the CPU and display memory is accomplished via a bidirectional latched port and is controlled by the PVTC signals read data buffer ($\overline{RDB}$), write data buffer ($\overline{WDB}$), and buffer chip enable ($\overline{BCE}$). This mode provides a non-contention type of operation that does not require address multiplexers. The CPU does not address the memory directly - the read or write operation is performed at the address contained in the cursor address register or the pointer address register as specified by the CPU. The PVTC enacts the data transfers during blanking intervals in order to prevent visual disturbances of the displayed data.

The CPU manages the data transfers by supplying commands to the PVTC. ,The commands used are:

1. Read/Write at pointer address.
2. Read/Write at cursor address (with optional increment of address).
3. Write from cursor address to pointer address.

The operational sequence for a write to memory operation is:

1. The CPU loads data to be written into the display memory into the interface latch.
2. The CPU writes the destination address into the PVTC's cursor or pointer registers.
3. The CPU checks the PVTC 'RDFLG' status bit to assure that any previous operation has been completed.
4. The CPU issues a 'write at cursor with/without increment' or a 'write at pointer' command to the PVTC.
5. The PVTC negates 'RDFLG', outputs the specified address, and generates control signals to perform requested operation. Data is copied from the interface latch into the memory.
6. The PVTC sets its 'RDFLG' status to indicate that the write operation is completed.

Similarly, a read operation proceeds as follows:

1. Steps 2 and 3 as above.
2. The CPU issues a 'read at cursor with/without increment' or 'read at pointer' command.
3. The PVTC negates 'RDFLG', outputs the specified address, and generates control signals to perform the read operation. Data is copied from the memory to the interface latch and the PVTC sets its 'RDFLG' status to indicate that the operation is completed.
4. The CPU checks the 'RDFLG' status to see if the read is completed.
5. The CPU reads the data from the interface latch.

Loading the same data into a block of display memory is accomplished via the 'write from cursor to pointer' command

1. The CPU loads the data to be written into the display memory into the interface latch.
2. The CPU writes the beginning address of the memory block into the PVTC's cursor address register and the ending address of the block into the pointer address register.
3. The CPU checks the 'RDFLG' status bit to assure that any previous operation has been completed.
4. The CPU issues a 'write from cursor to pointer' command to the PVTC.

INDEPENDENT BUFFER MODE CONFIGURATION

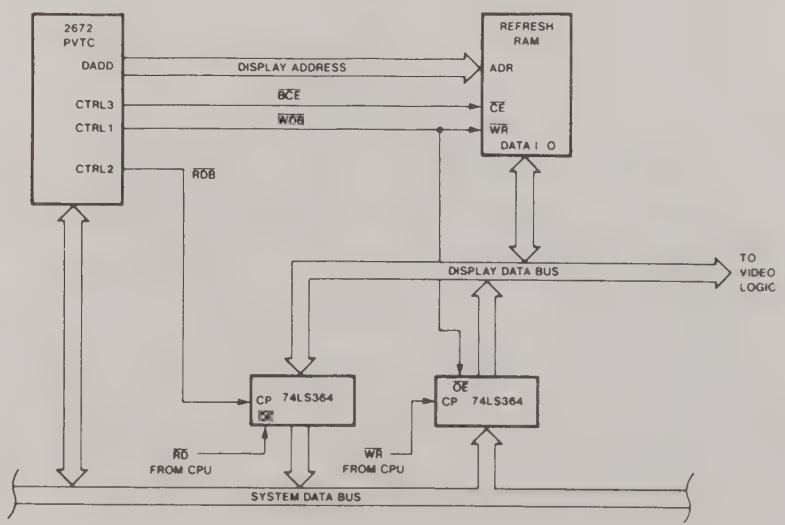

Figure 6

5. The PVTC negates 'RDFLG' and outputs block addresses and control signals to copy the data from the interface latch into the specified block of memory.
6. The PVTC sets its 'RDFLG' status to indicate that the block write is completed.

Similar sequences can be implemented on an interrupt driven basis using the READY interrupt output from the PVTC to inform the CPU that a previously requested command has been completed.

Two timing sequences are possible for the 'read/write at cursor/pointer' commands. If the command is given during the active display window (defined as first scan line of the first character row to the last scan line of the last character row), the operation takes place during the next horizontal blanking interval. If the command is given during the vertical blanking interval, or while the display has been commanded blanked, the operation takes place immediately.

For the 'write from cursor to pointer' operation, the PVTC's BLANK output is asserted automatically and remains asserted until the vertical retrace interval following completion of the command. The memory is filled at a rate of one location per two character times, plus a small amount of overhead.

Shared and Transparent Buffer Modes

In these modes the display buffer RAM is a part of the CPU memory domain and is addressed directly by the CPU. Both modes use the same hardware configuration with the CPU accessing the display buffer via three-state drivers (see figure 7). The processor bus request ($\overline{PBREQ}$) control signal informs the PVTC that the CPU is requesting access to the display buffer. In response to this request, the PVTC raises bus acknowledge ($\overline{BACK}$) until its bus external ($\overline{BEXT}$) output has freed the display address and data busses for CPU access. $\overline{BACK}$, which can be used as a 'hold' input to the CPU, is then lowered to indicate that the CPU can access the buffer.

In transparent mode, the PVTC delays the granting of the buffer to the CPU until a vertical or horizontal blanking interval, thereby causing minimum disturbance of the display. In shared mode, the PVTC will blank the display and grant immediate access to the CPU.

Row Buffer Mode

Figure 8 shows the hardware implementation for the row buffer mode. During the first scan line (line 0) of each character row, the PVTC halts the CPU and DMA's the next row of character data from the system memory to the row buffer memory. The PVTC then releases the CPU and displays the row buffer data for the programmed number of scan lines. The bus request ($\overline{BREQ}$) control signal informs the CPU that character addresses and the memory bus control (MBC) signal will start at the next falling edge of BLANK. The CPU must release the address and data busses before this time to prevent bus

PVTC SHARED OR TRANSPARENT BUFFER MODES

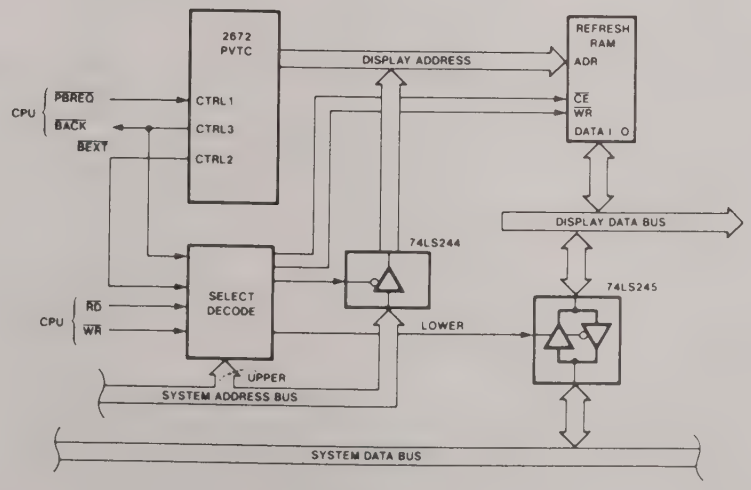

Figure 7

ROW BUFFER MODE CONFIGURATION

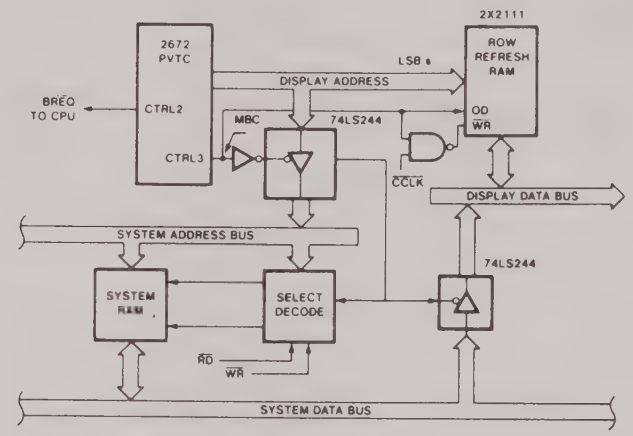

Figure 8

contention. After the row of character data is transferred to the CPU, BREQ returns high to grant memory control back to the CPU

A MINIMUM CHIP COUNT TERMINAL IMPLEMENTATION

Figure 9 is the schematic of a minimum chip count CRT terminal using the four CRT set devices. Only 15 IC packages are required for the complete implementation, including all keyboard encoding and RS-232 level conversion for the serial interface. Despite this low chip count the terminal is capable of providing an impressive array of features including:

Display Format:
- 24 or 25 character rows
- 80 characters per row

Character Format:
- 7x9 dot matrix character in a 9x12 character block
- 96 ASCII alphanumeric characters
- 32 special symbols
- Block graphics
- Line drawing character set

Cursor:
- Underline or block cursor
- Optional blinking

Keyboard:
- 128 keys maximum
- Non-encoded
- Cursor control keys
- Numeric keypad

Serial Interface:
- Full or half duplex
- RS-232 compatible
- 16 baud rates with internal baud rate generator
- Character or block transmission

Operating Modes:
- Normal
- Transparent (displays graphic and control characters)
- Page or scroll with optional smooth scroll

Visual Attributes:
- Blink
- Reverse video
- Highlight
- Underline
- Non-display

The system utilizes the independent buffer mode to minimize hardware requirements. The dual port interface to the 2Kx8 display buffer is via a Signetics 8X31 bidirectional latch. This may be replaced by a unidirectional latch such as the 74LS374 if reading of the RAM's contents by the CPU is not required.

The operating program for the terminal is contained in the internal ROM of the 8049 microcomputer, which also provides the RAM required by the system program. Since the majority of the terminal's features are tailored by firmware, the ROM size can be increased, either internally or externally, to support additional functions.[1]

BASIC TERMINAL SOFTWARE

The software for a microcomputer based terminal is closely tied to the system hardware configuration and its characteristics. If an interrupt driven mode of operation is desired, the system hardware/software design must be capable of prioritizing the interrupts so that the system will correctly service interrupts from different sources. In a typical system, there are three interrupt sources: the keyboard, the communications interface, and the video timing controller. The latter must usually be assigned the highest priority since failure to service an interrupt from the video timing controller on a timely basis may result in visual perturbations on the display. The keyboard and datacomm interrupts can, in most cases, absorb some time delay before they are serviced since they include one or more levels of data buffers.

[1]A pre-programmed 8049 microcomputer containing the operating firmware for this terminal will be available from Signetics.

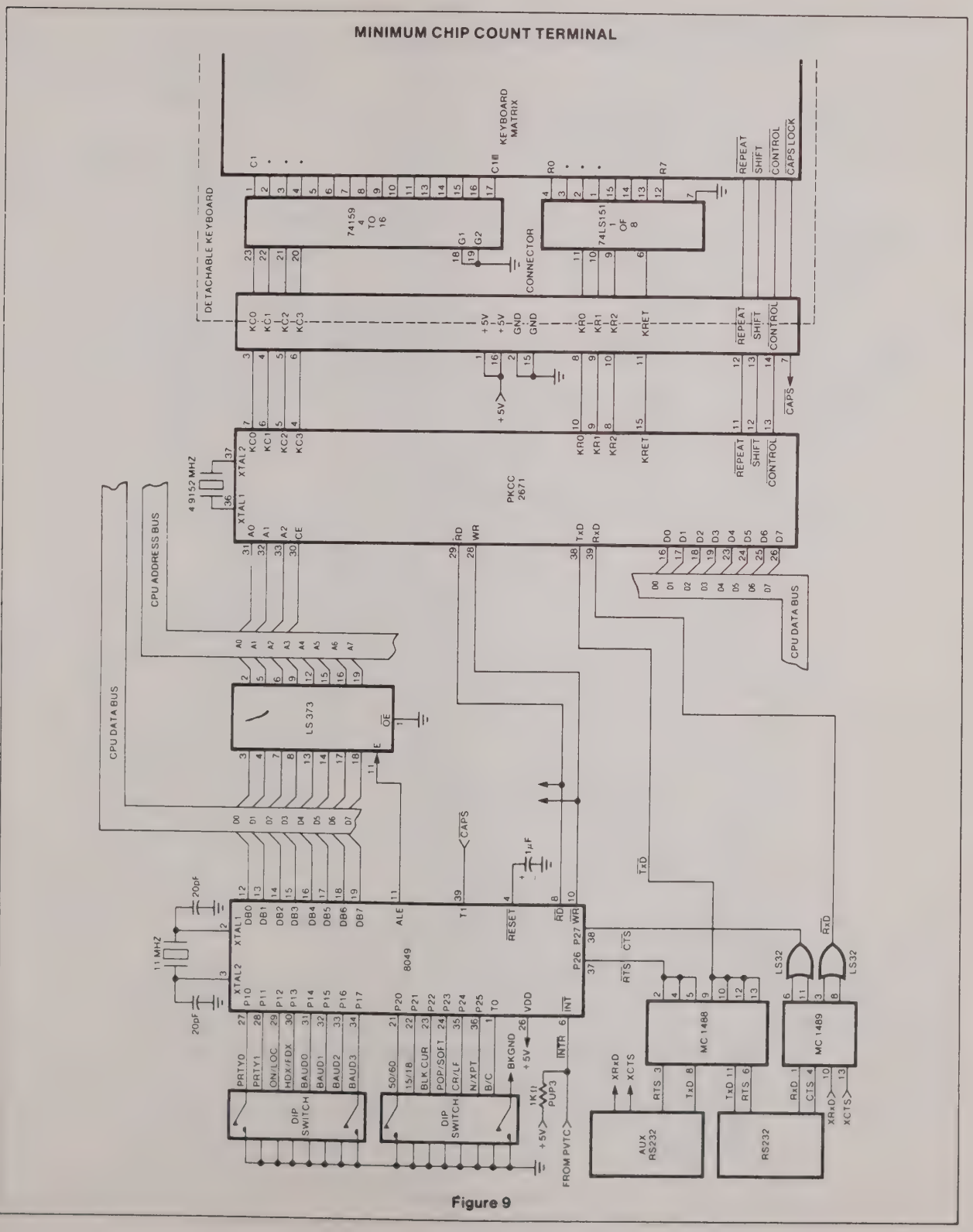
MINIMUM CHIP COUNT TERMINAL
DETACHABLE KEYBOARD
KEYBOARD MATRIX
CONNECTOR
74159 4 TO 16
74LS151 1 OF 8
REPEAT
SHIFT
CONTROL
CAPSLOCK
CAPS
PKCC 2671
4.9152 MHZ
CPU ADDRESS BUS
CPU DATA BUS
LS 373
11 MHZ
20pF
1μF
8049
DIP SWITCH
MC 1488
MC 1489
LS32
AUX RS232
RS232
FROM PVTC

Figure 9

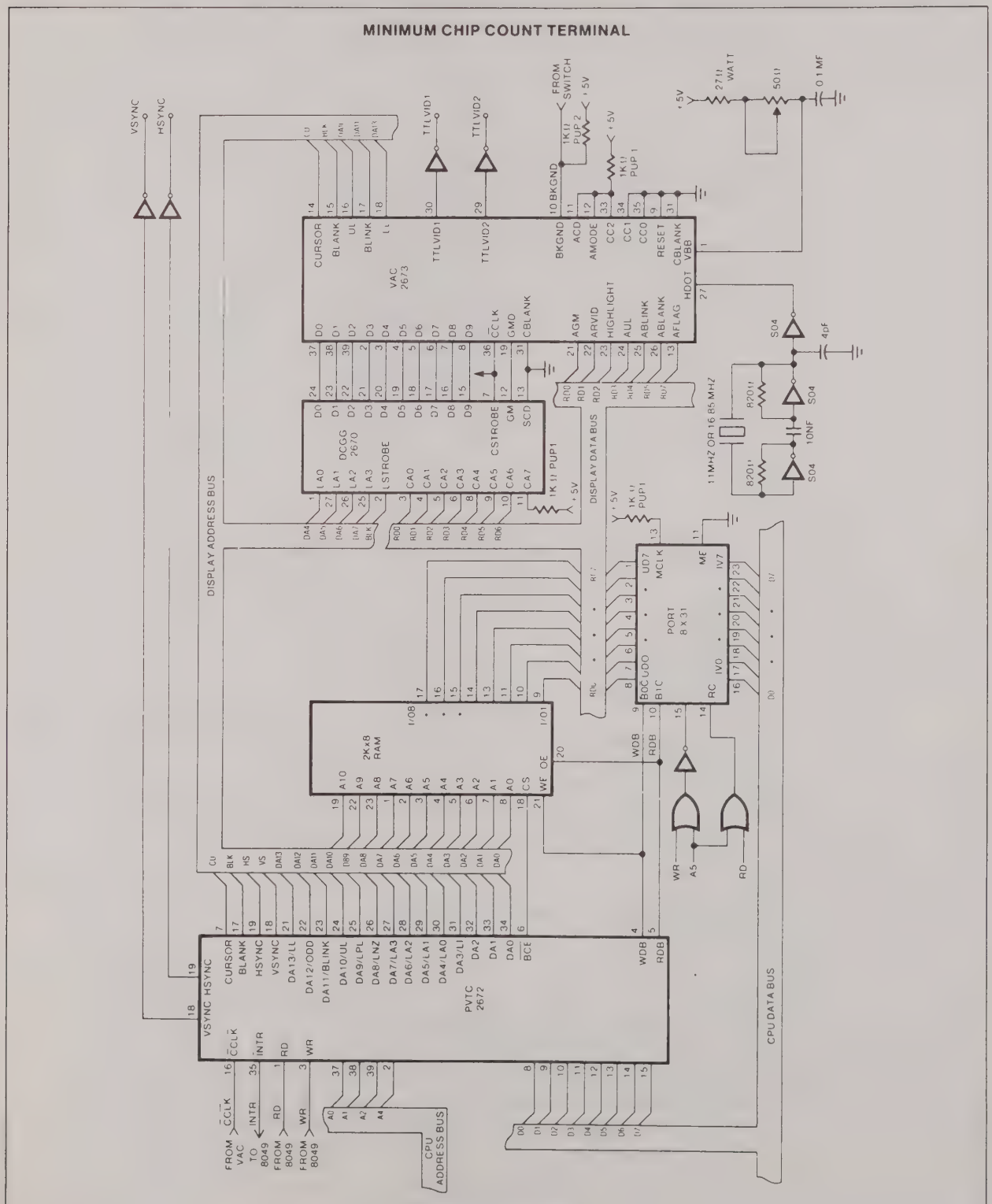

Figure 9 (Continued)

Often, a multi-level interrupt structure will be required so that a high priority interrupt requiring immediate service can be serviced even while the system is in the process of servicing a lower priority interrupt.

A simplified flowchart for the software for an interrupt driven terminal is shown in figure 10. After application of power, the microprocessor first performs a system initialization routine which consists of five parts

1. Clear the microcomputer's scratchpad RAM.
2. Initialize the 2672 PVTC for the desired screen format, monitor timing parameters, cursor parameters, and display start address.
3. Clear the CRT display by loading a non display-code (usually an ASCII 'space', 20 hex) into the buffer memory
4. Initialize the 2671 PKCC for the desired keyboard and serial interface modes.
5. Read any mode switches (e.g., full or half duplex, baud rate, cursor type, etc.) and set system parameters as required

The processor can now enable its interrupts and wait in a loop until an interrupt is received. When this happens, the processor first determines the source of the interrupt and then performs the required system operation.

An interrupt from the CRT timing controller usually indicates that some information is required for proper screen refresh operation. For example, the PVTC may issue a 'split screen' interrupt to indicate that a new address must be loaded into its screen start registers in order for the next character row to be displayed from other than the next sequential address in memory. The CPU must service this interrupt within a finite time in order for the display to operate correctly

An interrupt from the keyboard interface may be either a displayable character or a control function. Displayable characters are usually transmitted to the host computer and also placed into the buffer memory for display on the terminal. Certain control characters, such as cursor control keys or keyboard error codes, may cause only local actions, while others will also require transmission to the host

An interrupt from the data communications interface may also be a displayable character or a system control character. In either case the microprocessor must determine the type of character and perform the necessary system operation.

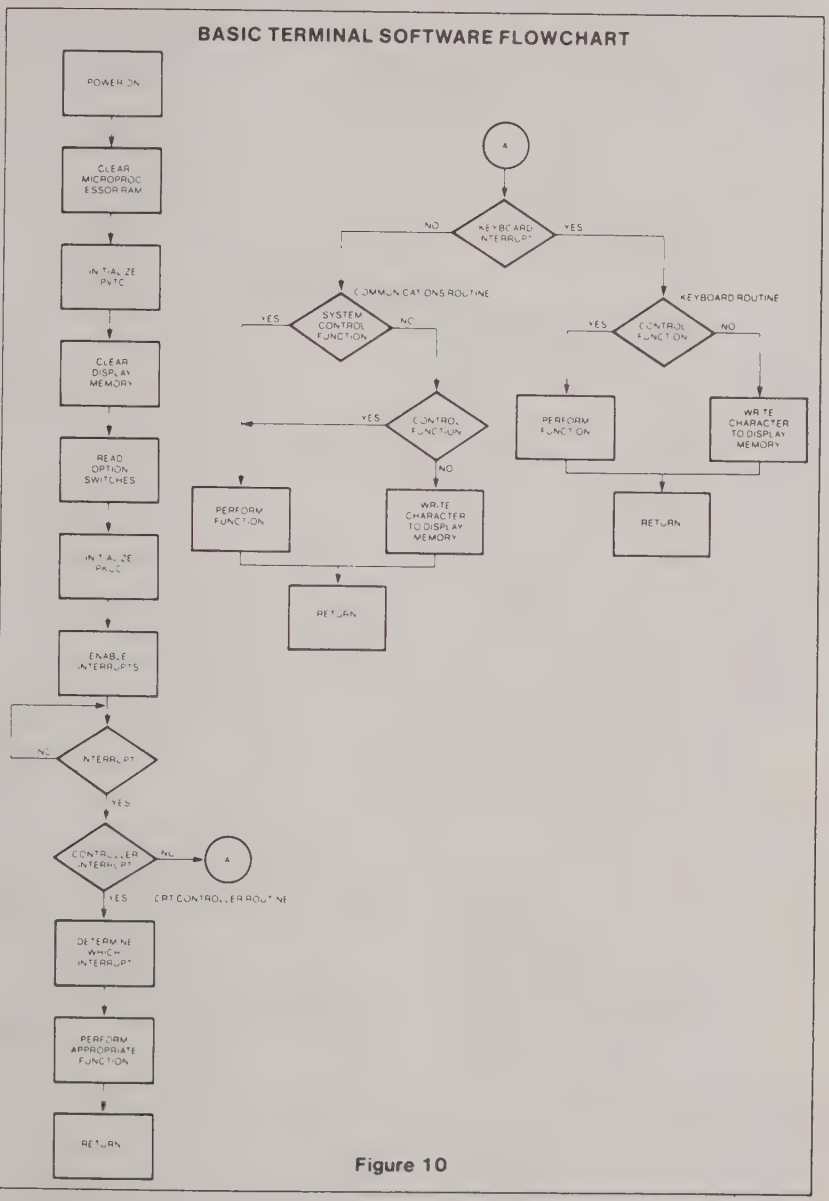

Figure 10

A DESIGN EXAMPLE

A fully operational emulation of an IBM 3101 terminal was designed and constructed using the Signetics CRT chip set. The terminal incorporates the majority of the 3101's functions. Selected functions were not incorporated due to program memory limitations. For example, the tabbing functions were developed and tested but were left out in deference to the block transmission functions. More features could have been included by selecting another of the numerous microprocessor devices on the market with greater program memory capacity. Major features of the terminal are summarized in table 1.[1]

[1]A data package for the design, including details of operation, schematic, and program listing, is available upon request by writing to:

Signetics Corporation
Microprocessor Applications Dept.
Mail Station 12-76
P.O. Box 409
Sunnyvale, CA 94086

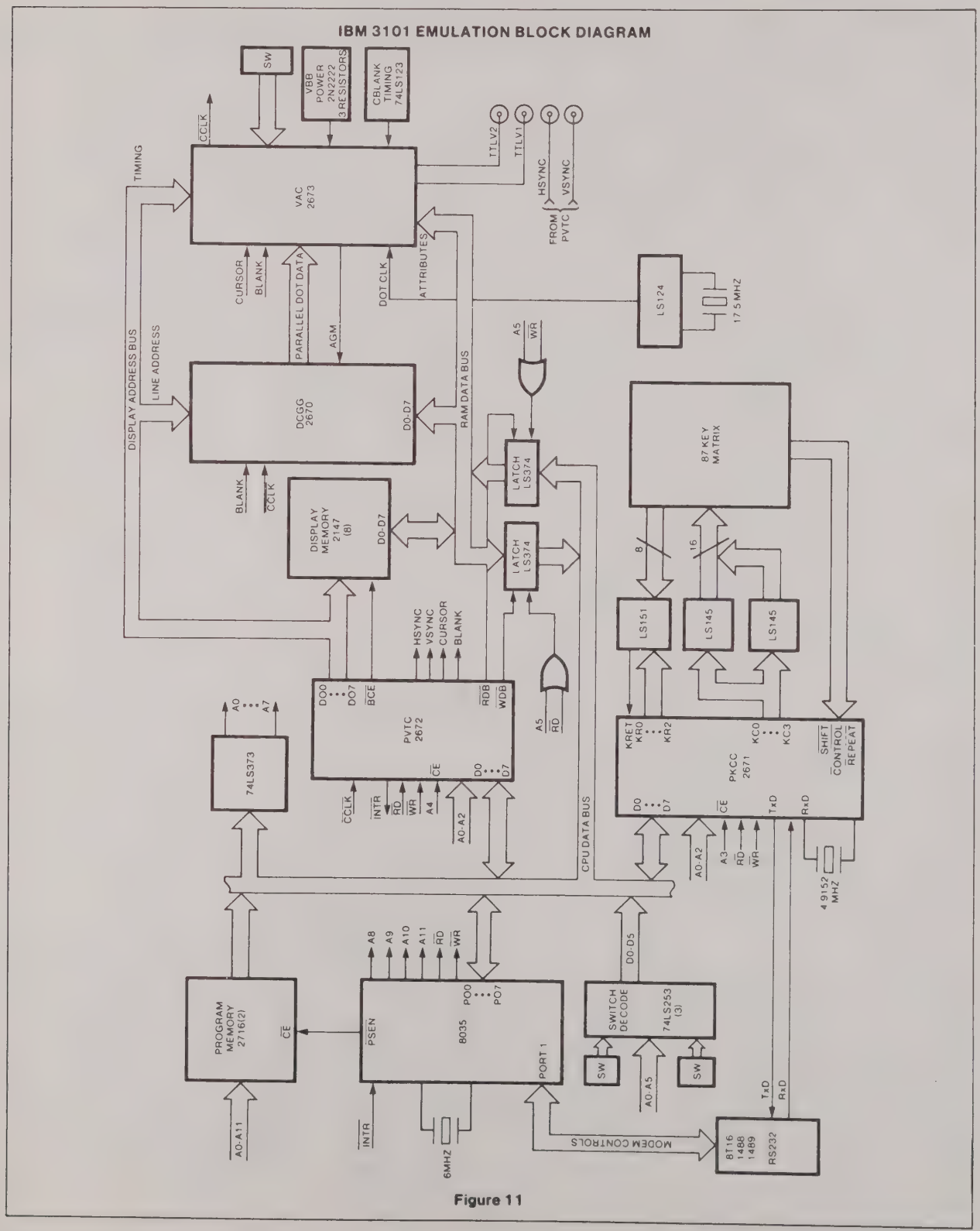
IBM 3101 EMULATION BLOCK DIAGRAM
SW
VBB POWER 2N2222 3 RESISTORS
CBLANK TIMING 74LS123
CCLK
TTLV2
TTLV1
HSYNC
VSYNC
FROM PVTC
TIMING
VAC 2673
CURSOR
BLANK
PARALLEL DOT DATA
AGM
DOT CLK
ATTRIBUTES
LS124
17.5 MHZ
DISPLAY ADDRESS BUS
LINE ADDRESS
DCGG 2670
D0-D7
RAM DATA BUS
A5
WR
LATCH LS374
87 KEY MATRIX
DISPLAY MEMORY 2147 (8)
8
16
LS151
LS145
LS145
HSYNC
VSYNC
CURSOR
BLANK
PVTC 2672
BCE
RDB
WDB
CE
RD
74LS373
A0 ... A7
INTR
A4
A0-A2
CPU DATA BUS
KRET
KR0 ... KR2
KC0 ... KC3
SHIFT
CONTROL
REPEAT
PKCC 2671
TxD
RxD
A3
49.152 MHZ
A8
A9
A10
A11
PROGRAM MEMORY 2716(2)
PSEN
8035
PO0 ... PO7
PORT 1
D0-D5
SWITCH DECODE
74LS253 (3)
SW
A0-A5
A0-A11
6MHZ
MODEM CONTROLS
BT.16 1488 1489 RS232

Figure 11

Table 1 — TERMINAL FEATURES

Display Screen Format
- 2000 character screen capacity (25 rows x 80 columns)
- Operator information area (25th line)
- Block-shaped cursor with optional blinking

Displayable Graphic Set
- 95 ASCII characters for non-transparent mode
- 128 characters for transparent mode
- 7x9 character matrix in 9x12 field

Keyboard
- 63-key main keyboard
- 12-key control key cluster
- 12-key numeric keypad
- Keyboard lock/unlock under software control
- Keyboard clicker
- Typamatic operation

Edit Functions
- Cursor controls: up, down, left, right, home
- Cursor address read and write
- Erase functions: erase EOL, erase EOS, clear screen

Visual Attributes
- Highlighted field
- Blinking field
- Non-displayed field
- Underlined field

Modes of Operation
- Transmission modes: character or block (page or line)
- Normal or transparent

Line Protocol
- Asynchronous
- 7-bit ASCII with programmable parity
- One or two stop bits
- Full or half duplex
- Online or local
- Programmable line turnaround character for block mode (EOT/ETX/CR/XOFF)
- EIA RS232 interface
- Communication line speed: 50 to 9,600 baud

Screen Refresh Rate
- 60 Hz

Terminal Hardware

The block diagram of the 8035 based terminal is illustrated in figure 11. It is an expanded version of the logic shown in figure 9, the major difference being a larger display RAM, to provide up to two pages of screen data, and the addition of several input ports to handle the large number of option and set-up switches. The terminal's software is contained in 4K of program storage external to the 8035.

The 2672 PVTC is programmed to operate in the independent buffer mode with the CPU isolated from the display RAM by two 74LS364 eight-bit latches, which provide the path for data transfers between the CPU and RAM. The PVTC, responding to commands from the CPU, completely controls the data transfer. To avoid display interference, the PVTC is instructed to complete the access during a blanking interval. For massive display updates (clear screen, load form, etc.) the PVTC is instructed to blank the display and service the data transfer immediately and continuously. Additional memory contention circuitry is not necessary since the PVTC provides all of the timing and addressing (via cursor and pointer) necessary to complete the transfer. An interrupt from the PVTC informs the CPU when an operation is completed.

The PVTC addresses the display buffer memory, which contains both character and attribute data. An attribute byte is identified by the software by setting bit 7 of the byte to a logic 1. The RAM data outputs are applied to the 2670 DCGG, which provides the character dot data information, and to the 2673 VAC.

The VAC is hardwired to operate in the field attributes mode for this application. An attribute character occupies a screen position but is not displayed unless the ACD input to the VAC is asserted. Bit 7 of the character byte identifies a character as an attribute character if it is a 1. When bit 7 on the RAM data bus is a 1, the attribute byte is latched into the VAC to begin a new attributes field. Since the attributes are double buffered in the VAC, only one byte (at any character position) is required to specify a field.

The bipolar VAC circuit serializes the dot data from the DCGG into a 17.5 MHz data stream for the monitor. Two TTL-level video outputs provide three levels of video: black, white, and gray.

The PKCC provides the asynchronous data communications link at one of sixteen selectable baud rates. The PKCC addresses two 74LS145s which act as a 4-to-16 decoder to drive a 16x8 matrix keyboard. Key depressions are detected on the KRET input from a 74LS151 8-to-1 multiplexer. Each key depression is debounced, encoded according to the states of the SHIFT and CONTROL inputs, and presented to the CPU. Repeat and 'typomatic' (auto-repeat) functions are processed automatically by the PKCC.

Timing Calculations

One of the tasks required in the design phase of the terminal is the selection of a suitable monitor and calculation of the PVTC register values to provide suitable drive signals for the selected monitor.

The selection process begins with calculation of the required horizontal scan frequency. Each character will be contained in a 9 dot by 12 line field. Since there are 25 display rows, the total number of active scan lines will be 12 x 25, or 300. To this we must add some number of scan lines for the vertical retrace, which is typically 5 to 10 percent of the active scan lines. For a screen refresh rate of 60 Hz, this yields

H frequency = (60)(300)(1.1) = 18,900 Hz.

A Motorola monitor was selected for the application. The major timing specifications for the monitor are:

Horizontal frequency: 18.72 KHz ± 500 Hz
Horizontal retrace: 8 us max
Horizontal sync width: 4 us min
Vertical frequency: 50/60 Hz
Vertical retrace: 750 us max
Vertical sync width: 50 us min

Monitor timing definitions are shown in figure 12. The worksheet illustrated in table 2 can be used to compute the required timing and associated PVTC register values. Some rough guesses are required initially and several iterations through the worksheet will usually be required to arrive at final values. For example, the character clock period must be known to select the horizontal front porch (HFP), sync width (HSYNC), and back porch (HBP) values. An estimate of the character period can be made initially as follows:

Horizontal period = 1/18,900 = 52.9 us
Horizontal active = total - blank = 52.9 — 10 = 42.9 us
Character period = 42.9/80 = 0.53 us approximately

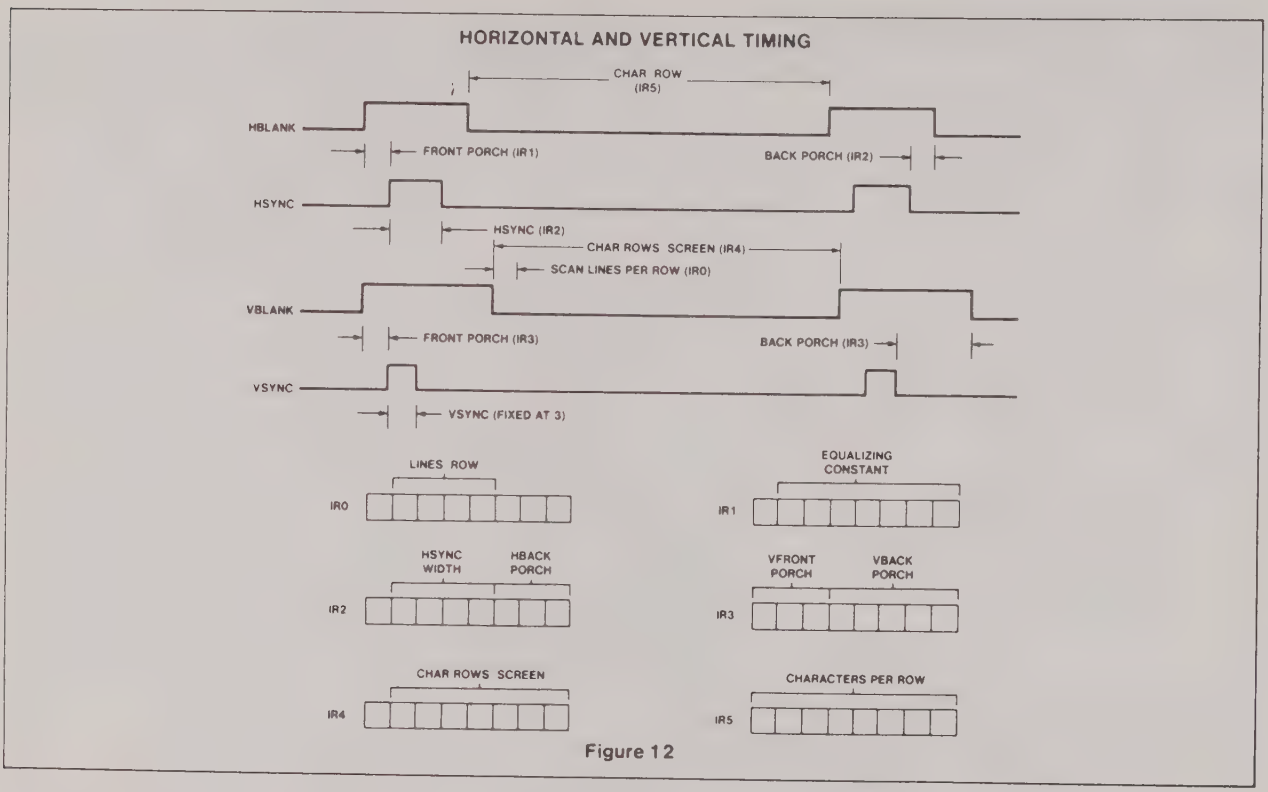

Figure 12

In calculating horizontal timing, an approximate ratio for the HFP, HSYNC, and HBP of 1:2:2 respectively is recommended.

Table 2 contains the final values selected for the application.

Memory Allocation

The 4K bytes of available buffer memory were allocated as follows (all addresses are in hex):

- 0000 to 004F: display data for row 25, status line
- 0050 to 0075: not used
- 0076 to 007F: CPU scratchpad
- 0080 to 07FF: display data for rows 1 to 24
- 0800 to 0FFF: not used, available for second page of display data

The PVTC's 'display buffer first address' and 'display buffer last address' registers are loaded with the values 0080 and 07FF respectively so as to cause this portion of the RAM to act as a circular buffer. Initially the display data is organized in the RAM as follows.

- 0080 to 00CF: row 1 data
- 00D0 to 011F: row 2 data

⋮

- 07B0 to 07FF: row 24 data

When a scroll operation is required, the CPU changes the value in the PVTC's 'screen start' register from 0080 to 00D0. This effectively shifts the displayed data up one row. Upon reaching the specified last buffer address (which is now the last character in row 23), the PVTC automatically changes the addressing sequence to resume starting at 0080 for the 24th row. The display data is now organized:

- 00D0 to 011F: row 1 data
- 0120 to 016F: row 2 data

⋮

- 07B0 to 07FF: row 23 data
- 0080 to 00CF: row 24 data

The CPU can clear the previous data in 0080 to 00CF so that a blank row appears in the 24th position.

The status line (row 25) data is kept in a separate section of RAM to eliminate the necessity of moving the data whenever the scrolling operation described above occurs. Thus, the PVTC must be instructed to change its addressing sequence at the beginning of the 25th row. This is accomplished by use of the split screen row interrupt capability. IR10, the 'split screen interrupt row' register, is initialized so as to cause an interrupt to be issued at the beginning of row 24. The CPU responds to this interrupt by changing the value in the screen start register to 0000. The PVTC then uses this value as the starting address of the next (25th) row, causing the status line to be displayed in that position. The CPU must re-load the screen start register before the end of the vertical blanking interval with the correct value for the first character to be displayed on the screen.

Terminal Software

Because the 8035 microcomputer used in the terminal provides only a single interrupt level, a totally interrupt driven software design could not be used. The interrupt was assigned to the PVTC to service the split screen interrupt described above and the operations required to implement the smooth scroll feature. The keyboard and datacomm functions are serviced by polling the PKCC status register. Both the keyboard interface and UART receiver are double buffered in the PKCC, preventing overrun even if they are not serviced immediately.

The program generally follows the typical program flow described previously. At system reset the 8035 interrupts are dis-

Table 2 — CRT TIMING WORKSHEET

1.	HORIZONTAL CHARACTER BLOCK (no. of dots)	9	
2.	VERTICAL CHARACTER BLOCK (no. of scan lines)	12	(IR0)
3.	VERTICAL REFRESH RATE, Hz	60	
4.	CHARACTERS PER ROW	80	(IR5)
5.	CHARACTER ROWS PER SCREEN	25	(IR4)
6.	TOTAL ACTIVE VIDEO SCAN LINES (step 2 x step 5)	300	
7.	VERTICAL FRONT PORCH (no. of scan lines)	4	(IR3)
8.	VERTICAL BACK PORCH (no. of scan lines)	12	(IR3)
9.	VERTICAL RETRACE INTERVAL (step 8 + 3)	15	
10.	TOTAL SCAN LINES PER FRAME (add steps 6, 7, and 9)	319	
11.	HORIZONTAL LINE RATE, KHz (step 3 x step 10)	19.14	
12.	HORIZONTAL FRONT PORCH (character time units)	5	
13.	HORIZONTAL SYNC WIDTH (character time units)	8	(IR2)
14.	HORIZONTAL BACK PORCH (character time units)	9	(IR2)
15	HORIZONTAL RETRACE INTERVAL (step 13 + step 14)	17	
16	TOTAL CHARACTER TIME UNITS IN ONE HORIZONTAL SCAN LINE (add steps 4, 12, 13, and 14)	102	
17	EQUALIZING CONSTANT ([step 16 / 2] — [2 x step 13])	35	(IR1)
18.	CHARACTER CLOCK RATE, MHz (step 16 x step 11)	1.95228	
19	CHARACTER PERIOD, us (1 / step 18)	0.512	
20	SCAN LINE PERIOD, us (step 19 x step 16)	53.27	
21.	DOT CLOCK RATE, MHz (step 18 x step 1)	17.57052	

	PARAMETER	SPEC	ACTUAL
A.	HORIZONTAL RATE, KHz	18.72 ± 0.5	19.14
B.	HORIZONTAL RETRACE TIME, us	8	8.7
C.	HORIZONTAL SYNC WIDTH	4	4.1
D.	VERTICAL RATE, Hz	50 - 60	60
E.	VERTICAL RETRACE TIME, us	750	784
F	VERTICAL SYNC WIDTH, us	50	157

abled, data memory and display memory are cleared to zeroes, and both the PVTC and PKCC are master reset through software commands. The system option switches are then read and stored and the PVTC and PKCC internal registers are initilized for the selected operation. Finally, the initial data for the status line is loaded, the PVTC, UART, and keyboard are enabled, and the CPU interrupt is enabled.

The program then enters a loop where the PKCC is checked for keyboard or UART entries. If an entry has occurred, the character is fetched and stored in a software controlled FIFO (first-in-first-out) memory which is eight bytes deep for both receiving or transmitting characters (the need for the FIFO is described below). If either FIFO has an entry, the program proceeds to a character recognition routine which checks for the type of character (displayable or control) and the appropriate handling subroutine (ESC sequence, control sequence, cursor control, character display, etc.) is called. If the FIFO's are empty, the polling routine checks the option switches for any changes since reset entry and if so reconfigures the system as necessary.

The need from the FIFOs results from the method used to effect the clear row function required when a scroll is performed. Although the PVTC includes a 'clear from cursor to pointer' command that can be used to clear a block of memory rapidly, the display is temporarily blanked during this operation. This would cause undesirable flashes on the display. Instead, the program does the function by a repetitive loop using the 'write at cursor and increment' command. Since the write occurs only once per scan line during the active display window, a worst case total of approximately 80 scan line times is required to execute the routine. This would limit the maximum received character rate to approximately one per 80 scan lines or about 240 characters per second (2400 baud). To overcome this limitation, the PKCC is also polled each time through the clear line subroutine loop, and any entries from the receiver or keyboard are stored in the appropriate FIFO. Since the FIFO is eight deep, this allows eight characters to be received in the same time, increasing the maximum baud rate to 19,200. (Other program limitations actually reduce the maximum baud rate to 9600 baud). However, this does not increase the rate at which characters which cause a scroll function to occur, such as a line feed, can be received. Each character of this type must be followed by 'fill' characters in order for data rates higher than 2400 baud to be used.

An interrupt from the PVTC will occur when the display scan reaches the row count programmed in its split screen address register, row address 24 (for the 24th row). In response to the interrupt, the CPU loads the screen start registers with the address of the status line (0000) and enables the PVTC's line zero interrupt. This causes another interrupt at the beginning of display of the status line. At this time the CPU reloads the screen start register with the proper address to begin the next display frame and disables the line zero interrupt.

If scrolling is required the screen start register value is incremented by 80 (popping off the top row) and the effective bottom row cleared to nulls. If soft scrolling is

selected, additional functions are performed during the interrupt routines. To begin the operation, the line zero interrupt routine adds ten lines to the vertical back porch. This causes the next active screen display to begin ten scan lines later than normal and gives the effect of the display moving up two scan lines (12 lines per character row - 10) instead of jumping up 12 lines. If nothing else were changed, however, the bottom of the display would move down ten lines. Thus, during the row 24 interrupt the number of scan lines per character row is changed to two (12-10), causing only the first two scan lines of that row to be shown. The next line zero interrupt (at row 25) restores the lines per row count back to 12 to keep the whole status line showing, and now changes the vertical back porch to 8. The display moves up two more scan lines and at the next row 24 interrupt four scan lines are shown. The process continues in this manner, providing the effect of the entire display, except for the status line, smoothly scrolling up over a selected interval of six frames, or one tenth of a second.

signetics

a subsidiary of U.S. Philips Corporation

Signetics Corporation
811 East Arques Avenue
P.O. Box 409
Sunnyvale, California 94086
Telephone 408/739-7700

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15M0481

NEC

μPD416
μPD416-1
μPD416-2
μPD416-3
μPD416-5

16384 x 1 BIT DYNAMIC MOS RANDOM ACCESS MEMORY

DESCRIPTION

The NEC μPD416 is a 16384 words by 1 bit Dynamic MOS RAM. It is designed for memory applications where very low cost and large bit storage are important design objectives.

The μPD416 is fabricated using a double-poly-layer N channel silicon gate process which affords high storage cell density and high performance. The use of dynamic circuitry throughout, including the sense amplifiers, assures minimal power dissipation.

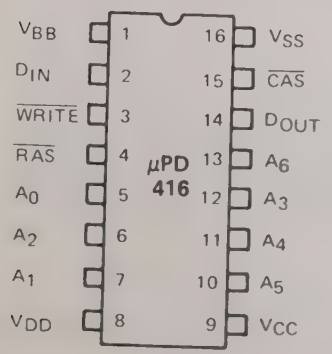
Multiplexed address inputs permit the μPD416 to be packaged in the standard 16 pin dual-in-line package. The 16 pin package provides the highest system bit densities and is available in either ceramic or plastic. Noncritical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

FEATURES

- 16384 Words x 1 Bit Organization
- High Memory Density — 16 Pin Ceramic and Plastic Packages
- Multiplexed Address Inputs
- Standard Power Supplies +12V, −5V, +5V
- Low Power Dissipation; 462 mW Active (MAX), 20 mW Standby (MAX)
- Output Data Controlled by $\overline{CAS}$ and Unlatched at End of Cycle
- Read-Modify-Write, $\overline{RAS}$-only Refresh, and Page Mode Capability
- All Inputs TTL Compatible, and Low Capacitance
- 128 Refresh Cycles
- 5 Performance Ranges:

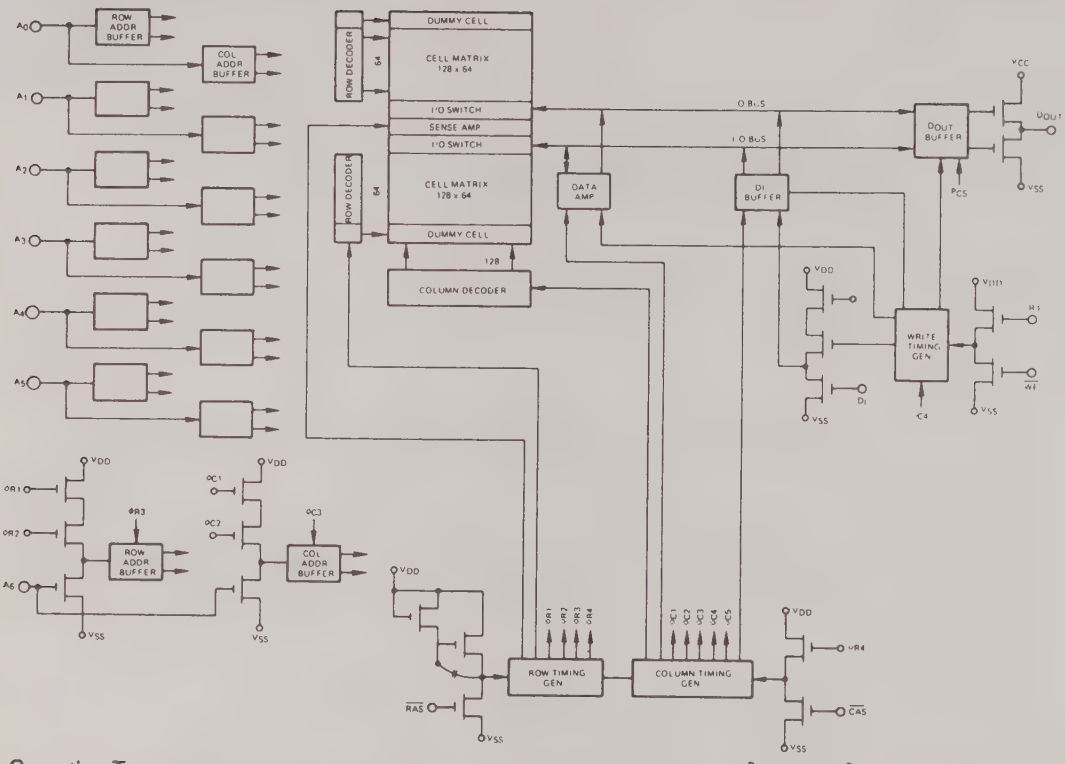
	ACCESS TIME	R/W CYCLE	RMW CYCLE
μPD416	300 ns	510 ns	575 ns
μPD416-1	250 ns	410 ns	465 ns
μPD416-2	200 ns	375 ns	375 ns
μPD416-3	150 ns	375 ns	375 ns
μPD416-5	120 ns	320 ns	320 ns

PIN CONFIGURATION



A_0-A_6	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write
V_{BB}	Power (-5V)
V_{CC}	Power (+5V)
V_{DD}	Power (+12V)
V_{SS}	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +150°C
All Output Voltages ①	−0.5 to +20 Volts
All Input Voltages ①	−0.5 to +20 Volts
Supply Voltages V_{DD}, V_{CC}, V_{SS} ①	−0.5 to +20 Volts
Supply Voltages V_{DD}, V_{CC} ②	−1.0 to +15 Volts
Short Circuit Output Current	50 mA
Power Dissipation	1 Watt

Notes: ① Relative to V_{BB}
② Relative to V_{SS}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

CAPACITANCE

T_a = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{BB} = −5V ± 10%, V_{CC} = +5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance (A_0-A_6), D_{IN}	C_{I1}		4	5	pF	
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}		8	10	pF	
Output Capacitance (D_{OUT})	C_O		5	7	pF	

DC CHARACTERISTICS

T_a = 0°C to +70°C ①, V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Supply Voltage	V_{DD}	10.8	12.0	13.2	V	②
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	② ③
Supply Voltage	V_{SS}	0	0	0	V	②
Supply Voltage	V_{BB}	− 4.5	−5.0	-5.5	V	②
Input High (Logic 1) Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IHC}	2.7		7.0	V	②
Input High (Logic 1) Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$ $\overline{WRITE}$	V_{IH}	2.4		7.0	V	②
Input Low (Logic 0) Voltage, all inputs	V_{IL}	− 1.0		0.8	V	②
Operating V_{DD} Current	I_{DD1}			35	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} Min. ④
Standby V_{DD} Current	I_{DD2}			1.5	mA	$\overline{RAS}$ = V_{IHC}; D_{OUT} = High Impedance
Refresh V_{DD} Current — All Speeds except μPD416-5	I_{DD3}			25	mA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}; t_{RC} = 375 ns ④
Refresh V_{DD} Current — μPD416-5	I_{DD3}			27	mA	
Page Mode V_{DD} Current	I_{DD4}			27	mA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = 225 ns ④
Operating V_{CC} Current	I_{CC1}				μA	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = 375 ns ⑤
Standby V_{CC} Current	I_{CC2}	-10		10	μA	$\overline{RAS}$ = V_{IHC}, D_{OUT} = High Impedance
Refresh V_{CC} Current	I_{CC3}	−10		10	μA	$\overline{RAS}$ cycling, $\overline{CAS}$ - V_{IHC}, t_{RC} 375 ns
Page Mode V_{CC} Current	I_{CC4}				μA	$\overline{RAS}$ V_{IL}, $\overline{CAS}$ cycling, t_{PC} 225 ns ⑤
Operating V_{BB} Current	I_{BB1}			200	μA	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} 375 ns
Standby V_{BB} Current	I_{BB2}			100	μA	$\overline{RAS}$ V_{IHC}, D_{OUT} High Impedance
Refresh V_{BB} Current	I_{BB3}			200	μA	$\overline{RAS}$ cycling, $\overline{CAS}$ - V_{IHC}, t_{RC} = 375 ns
Page Mode V_{BB} Current	I_{BB4}			200	μA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = 225 ns
Input Leakage (any input)	$I_{I(L)}$	−10		10	μA	V_{BB} = -5V, 0V ≤ V_{IN} ≤ +7V, all other pins not under test = 0V
Output Leakage	$I_{O(L)}$	-10		10	μA	D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ +5.5V
Output High Voltage (Logic 1)	V_{OH}	2.4			V	I_{OUT} = −5 mA ③
Output Low Voltage (Logic 0)	V_{OL}			0.4	V	I_{OUT} 4 2 mA

Notes: ① T_a is specified here for operation at frequencies to t_{RC} ≥ t_{RC} (min). Operation at higher cycle rates with reduced ambient temperatures and high power dissipation is permissible, however, provided AC operating parameters are met See Figure 1 for derating curve.

② All voltages referenced to V_{SS}.

③ Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.

④ I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate. See Figures 2, 3 and 4 for I_{DD} limits at other cycle rates.

⑤ I_{CC1} and I_{CC4} depend upon output loading. During readout of high level data V_{CC} is connected through a low impedance (135Ω typ) to data out. At all other times I_{CC} consists of leakage currents only

DERATING CURVES

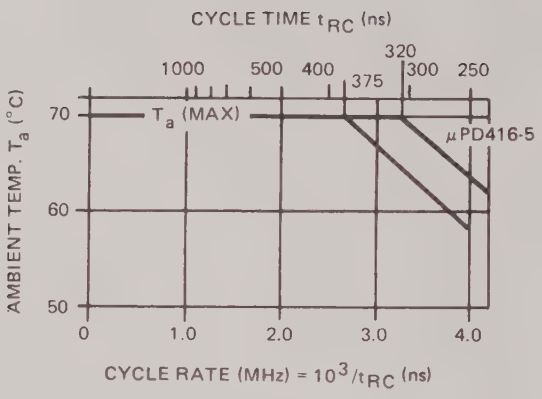


FIGURE 1

Maximum ambient temperature versus cycle rate for extended frequency operation. T_a (max) for operation at cycling rates greater than 2.66 MHz ($t_{CYC} < 375$ ns) is determined by T_a (max) [°C] = 70 – 9.0 x (cycle rate [MHz] –2.66). For μPD416-5, it is T_a (max) [°C] = 70 – 9.0 (cycle rate [MHz] – 3.125).

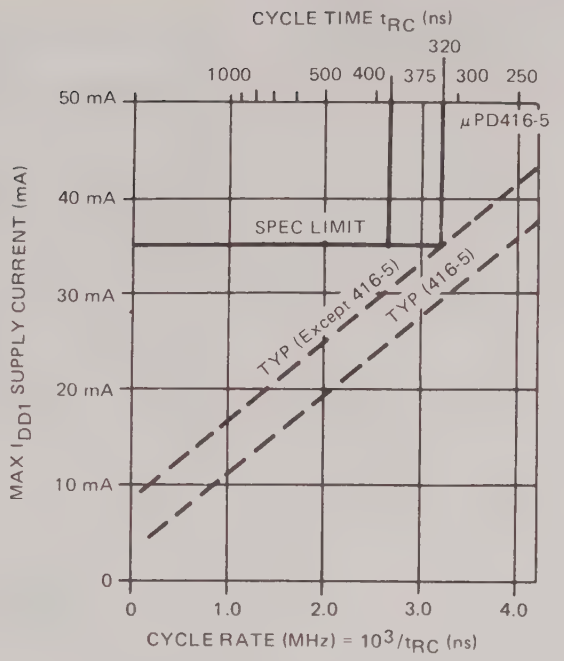


FIGURE 2

Maximum I_{DD1} versus cycle rate for device operation at extended frequencies.

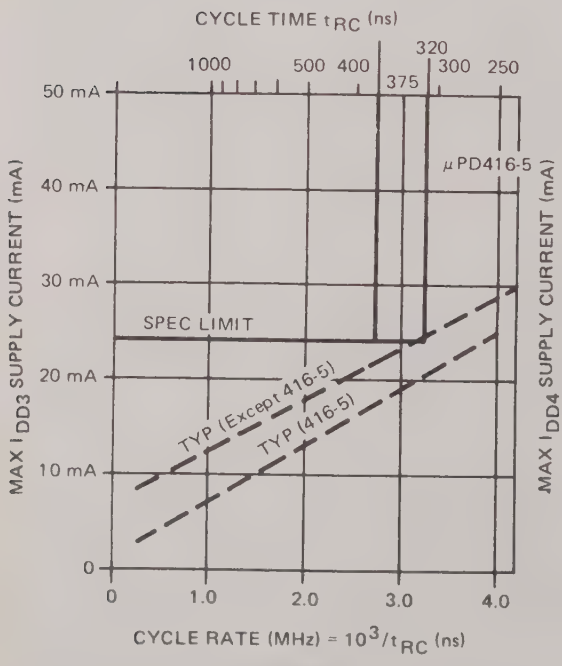


FIGURE 3

Maximum I_{DD3} versus cycle rate for device operation at extended frequencies.

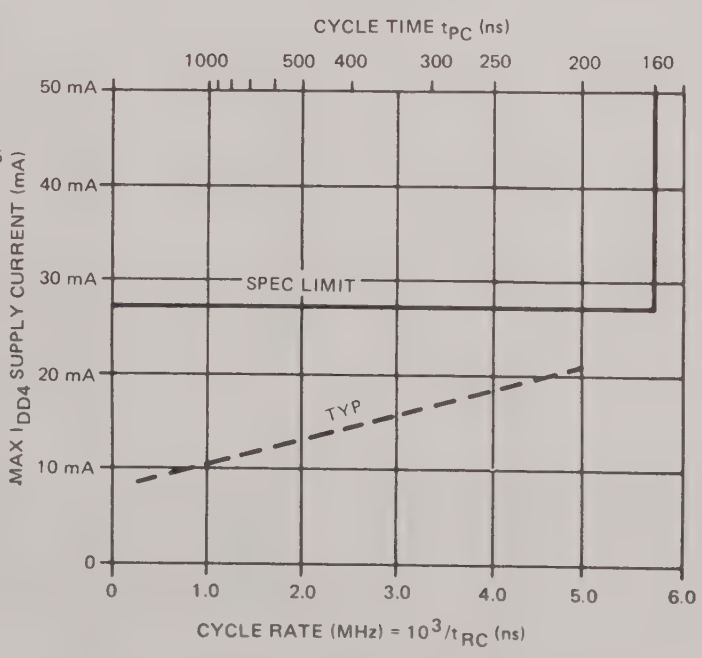


FIGURE 4

Maximum I_{DD4} versus cycle rate for device operation in page mode.

AC CHARACTERISTICS

T_a = 0°C to +70°C, V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS										UNIT	TEST CONDITIONS
		μPD416		μPD416-1		μPD416-2		μPD416-3		μPD416-5			
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Random read or write cycle time	t_{RC}	510		410		375		375		320		ns	③
Read-write cycle time	t_{RWC}	575		465		375		375		320		ns	③
Page mode cycle time	t_{PC}	330		275		225		170		160		ns	
Access time from $\overline{RAS}$	t_{RAC}		300		250		200		150		120	ns	④ ⑥
Access time from $\overline{CAS}$	t_{CAC}		200		165		135		100		80	ns	⑤ ⑥
Output buffer turn-off delay	t_{OFF}	0	80	0	60	0	50	0	40	0	35	ns	⑦
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	35	3	35	ns	②
$\overline{RAS}$ precharge time	t_{RP}	200		150		120		100		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	300	10,000	250	10,000	200	32,000	150	32,000	120	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	200		165		135		100		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	200	10,000	165	10,000	135	10,000	100	10,000	80	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	40	100	35	85	25	65	20	50	15	40	ns	⑧
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	−20		−20		−20		−20		0		ns	
Row address set-up time	t_{ASR}	0		0		0		0		0		ns	
Row address hold time	t_{RAH}	40		35		25		20		15		ns	
Column address set-up time	t_{ASC}	10		10		−10		−10		−10		ns	
Column address hold time	t_{CAH}	90		75		55		45		40		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	190		160		120		95		80		ns	
Read command set-up time	t_{RCS}	0		0		0		0		0		ns	
Read command hold time	t_{RCH}	0		0		0		0		0		ns	
Write command hold time	t_{WCH}	90		75		55		45		40		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	190		160		120		95		80		ns	
Write command pulse width	t_{WP}	90		75		55		45		40		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	120		100		80		60		60		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	120		100		80		60		60		ns	
Data-in set-up time	t_{DS}	0		0		0		0		0		ns	⑨
Data-in hold time	t_{DH}	90		75		55		45		40		ns	⑨
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	190		160		120		95		80		ns	
CAS precharge time (for page mode cycle only)	t_{CP}	120		100		80		60		60		ns	
Refresh period	t_{REF}		2		2		2		2		2	ms	
$\overline{WRITE}$ command set-up time	t_{WCS}	20		−20		20		20		0		ns	⑩
$\overline{CAS}$ to $\overline{WRITE}$ delay	t_{CWD}	140		125		95		70		80		ns	⑩
$\overline{RAS}$ to $\overline{WRITE}$ delay	t_{RWD}	240		200		160		120		120		ns	⑩

Notes:

① AC measurements assume t_T = 5 ns.

② V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}

③ The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_a ≤ 70°C) is assured

④ Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.

⑤ Assumes that $t_{RCD} \geq t_{RCD}$ (max).

⑥ Measured with a load equivalent to 2 TTL loads and 100 pF

⑦ t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels

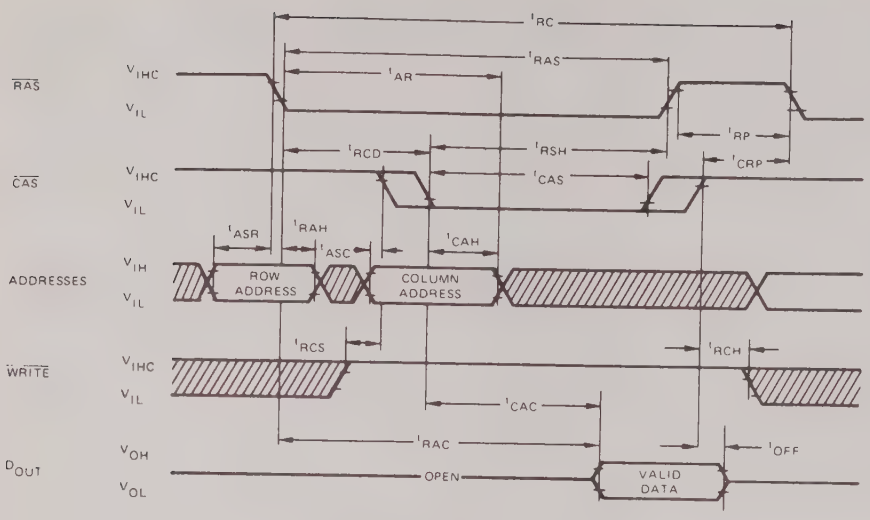
⑧ Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

⑨ These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles

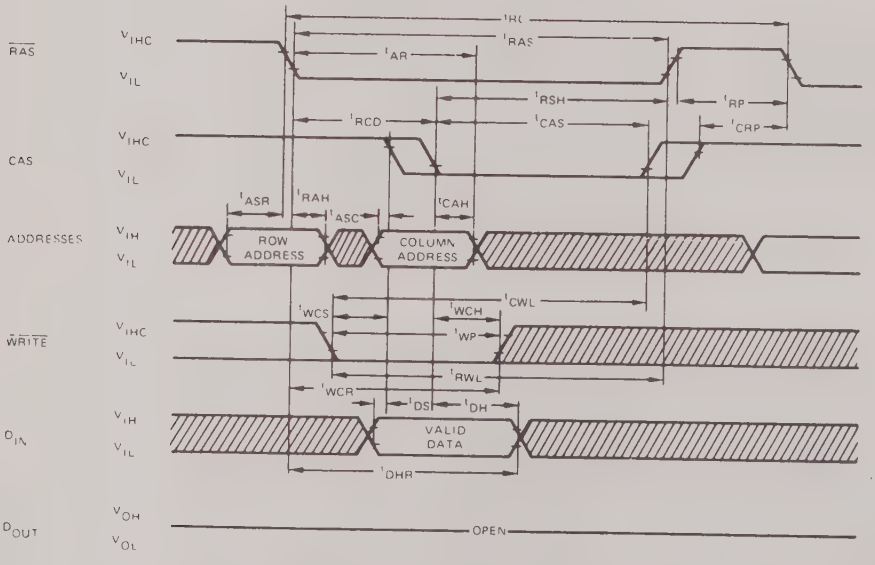
⑩ t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) $\geq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate

TIMING WAVEFORMS

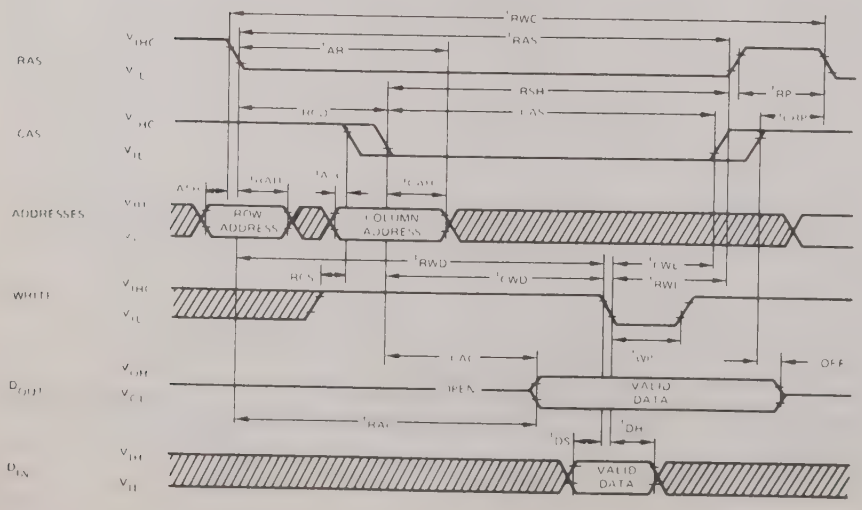
READ CYCLE



WRITE CYCLE

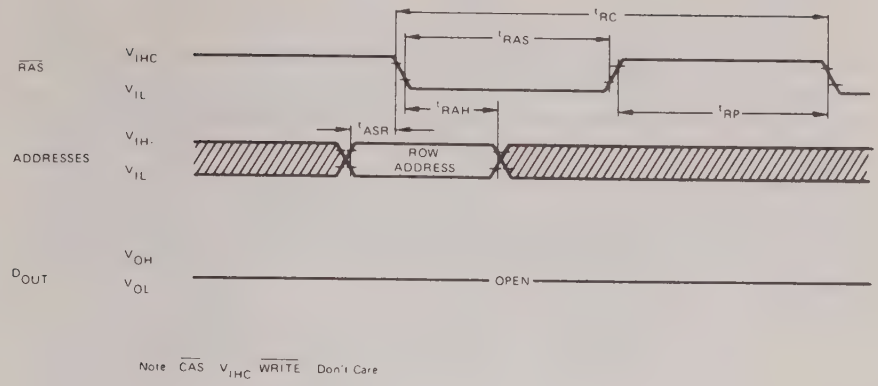


READ-WRITE/READ-MODIFY-WRITE CYCLE



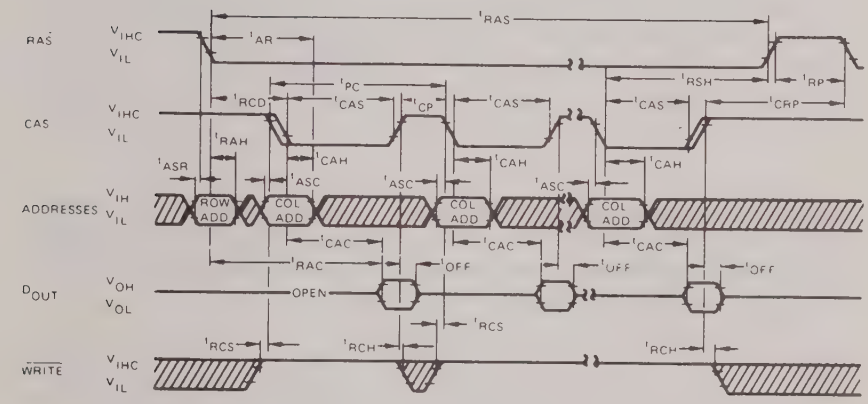
TIMING WAVEFORMS (CONT.)

"$\overline{RAS}$-ONLY" REFRESH CYCLE

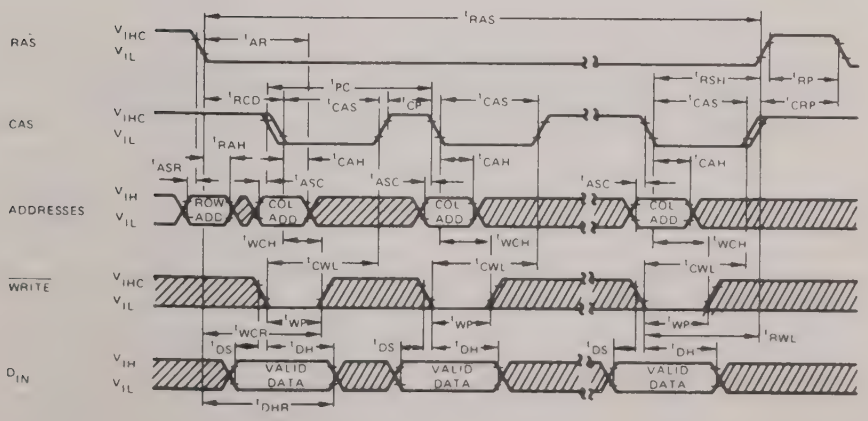


Note $\overline{CAS}$ V_{IHC} $\overline{WRITE}$ Don't Care

PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



ADDRESSING

The 14 address bits required to decode 1 of 16,384 bit locations are multiplexed onto the 7 address pins and then latched on the chip with the use of the Row Address Strobe ($\overline{RAS}$), and the Column Address Strobe ($\overline{CAS}$). The 7 bit row address is first applied and $\overline{RAS}$ is then brought low. After the $\overline{RAS}$ hold time has elapsed, the 7 bit column address is applied and $\overline{CAS}$ is brought low. Since the column address is not needed internally until a time of t_{CRD} MAX after the row address, this multiplexing operation imposes no penalty on access time as long as $\overline{CAS}$ is applied no later than t_{CRD} MAX. If this time is exceeded, access time will be defined from $\overline{CAS}$ instead of $\overline{RAS}$.

DATA I/O

For a write operation, the input data is latched on the chip by the negative going edge of $\overline{WRITE}$ or $\overline{CAS}$, whichever occurs later. If $\overline{WRITE}$ is active before $\overline{CAS}$, this is an "early WRITE" cycle and data out will remain in the high impedance state throughout the cycle. For a READ, WRITE, OR READ-MODIFY-WRITE cycle, the data output will contain the data in the selected cell after the access time. Data out will assume the high impedance state anytime that $\overline{CAS}$ goes high.

PAGE MODE

The page mode feature allows the μPD416 to be read or written at multiple column addresses for the same row address. This is accomplished by maintaining a low on $\overline{RAS}$ and strobing the new column addresses with $\overline{CAS}$. This eliminates the setup and hold times for the row address resulting in faster operation.

REFRESH

Refresh of the memory matrix is accomplished by performing a memory cycle at each of the 128 row addresses every 2 milliseconds or less. Because data out is not latched, "$\overline{RAS}$ only"-cycles can be used for simple refreshing operation.

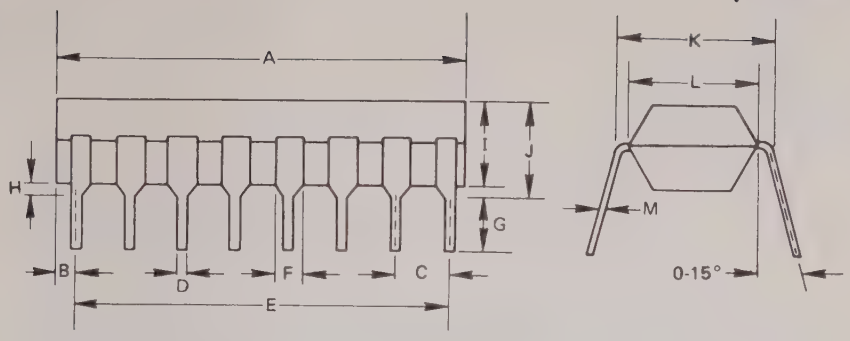
CHIP SELECTION

Either $\overline{RAS}$ and/or $\overline{CAS}$ can be decoded for chip select function. Unselected chip outputs will remain in the high impedance state.

POWER SEQUENCING

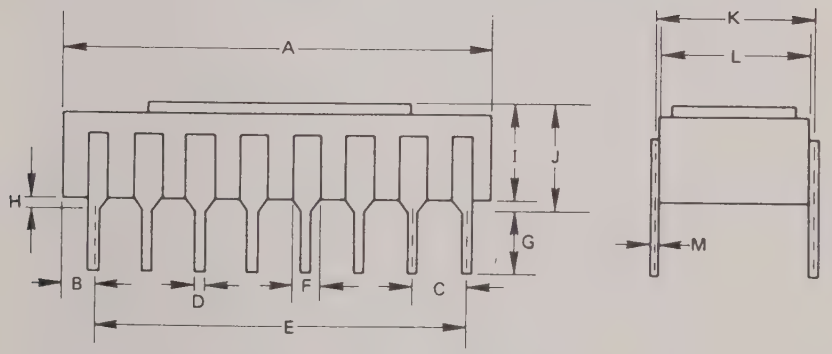
In order to assure long term reliability, V_{BB} should be applied first during power up and removed last during power down.

PACKAGE OUTLINE
μPD416C/D



μPD416C
(Plastic)

ITEM	MILLIMETERS	INCHES
A	19.4 MAX.	0.76 MAX.
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.05 MAX.	0.16 MAX.
J	4.55 MAX.	0.18 MAX.
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{0.05}$	0.01



μPD416D
(Ceramic)

ITEM	MILLIMETERS	INCHES
A	20.5 MAX.	0.81 MAX.
B	1.36	0.05
C	2.54	0.10
D	0.5	0.02
E	17 78	0.70
F	1.3	0.051
G	3.5 MIN.	0.14 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.20 MAX.
K	7.6	0.30
L	7.3 .	0.29
M	0.27	0.01

NEC
μPD444/6514
μPD444/6514-1
μPD444/6514-2
μPD444/6514-3

1024 × 4 BIT STATIC CMOS RAM

DESCRIPTION

The μPD444/6514 is a high speed, low power, silicon gate CMOS 4096 bit static RAM organized 1024 words by 4-bits. It uses fully DC stable (static) circuitry throughout and therefore requires no clock or refreshing to operate. Data access is particularly simple since address setup times are not required. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

$\overline{CS}$ controls the power down feature. In less than a cycle time after $\overline{CS}$ goes high – deselecting the μPD444/6514 – the part automatically reduces its power requirements and remains in this low power standby mode as long as $\overline{CS}$ remains high. There is no minimum $\overline{CS}$ high time for device operation, although it will determine the length of time in the power down mode. When $\overline{CS}$ goes low, selecting the μPD444/6514, the μPD444/6514 automatically powers up.

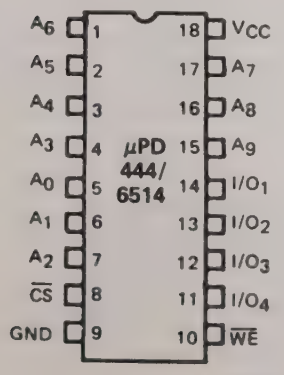
The μPD444/6514 is placed in an 18-pin plastic package for the highest possible density. It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. The μPD444/6514 is pin compatible with the μPD2114L NMOS Static RAM.

Data Retention is guaranteed to 2 volts on all parts. These devices are ideally suited for low power applications where battery operation or battery backup for non-volatility are required.

FEATURES

- Low Power Standby – 5 μW Typ.
- Low Power Operation
- Data Retention – 2.0V Min.
- Capability of Battery Backup Operation
- Fast Access Time – 200-450 ns
- Identical Cycle and Access Times
- Single +5V Supply
- No Clock or Timing Strobe Required
  Completely Static Memory
- Automatic Power-Down
- Directly TTL compatible: All Inputs and Outputs
- Common Data Input and Output using Three-State Outputs
- Replacement for μPD2114L and Equivalent Devices
- Available in a Standard 18-Pin Plastic Package

PIN CONFIGURATION

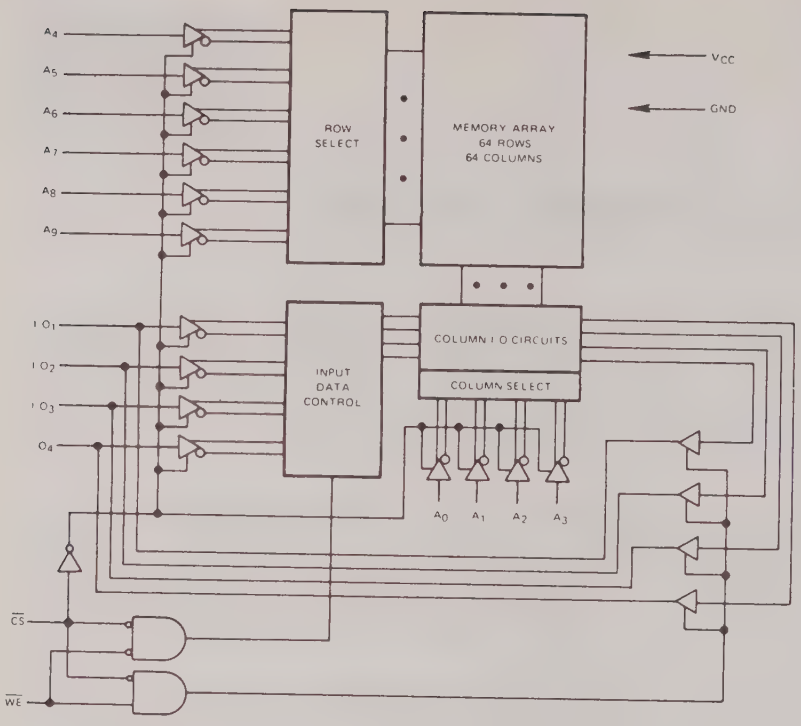


PIN NAMES

A_0-A_9	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
I/O_1-I/O_4	Data Input/Output
V_{CC}	Power (+5V)
GND	Ground

Rev/1

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−40°C to +85°C
Storage Temperature	−55°C to +125°C
All Input and Output Voltages	−0.3 to V_{CC} +0.3 Volts ①
Supply Voltage	+8.0 Volts

Note: ① With Respect to Ground

COMMENT Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

*T_a = 25°C

DC CHARACTERISTICS

T_a = −40°C to +85°C; V_{CC} = +5V ± 10% unless otherwise tested

PARAMETER	SYMBOL	LIMITS 444/6514-3 MIN	444/6514-3 TYP	444/6514-3 MAX	444/6514-2 MIN	444/6514-2 TYP	444/6514-2 MAX	444/6514-1 MIN	444/6514-1 TYP	444/6514-1 MAX	444/6514 MIN	444/6514 TYP	444/6514 MAX	UNIT	TEST CONDITIONS
Input Leakage Current	I_{LI}	−1.0		1.0	−1.0		1.0	−1.0		1.0	−1.0		1.0	μA	V_{IN} = GND to V_{CC}
I/O Leakage Current	I_{LO}	−1.0		1.0	−1.0		1.0	−1.0		1.0	−1.0		1.0	μA	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = GND to V_{CC}
Operating Supply Current	I_{CCA1}		20	35		18	35		16	35		14	35	mA	$\overline{CS}$ = V_{IL}, V_{IN} = V_{CC}, Outputs Open
Operating Supply Current	I_{CCA2}		24	40		22	40		19	40		17	40	mA	$\overline{CS}$ = V_{IL}, V_{IN} = 2.4V, Outputs Open
Average Operating Supply Current	I_{CCA3}		10			9			8			7		mA	V_{IN} = GND or V_{CC}, Outputs Open f = 1 MHz, Duty 50%
Standby Supply Current	I_{CCS}			50			50			50			50	μA	$\overline{CS}$ = V_{CC}, V_{IN} = GND to V_{CC}
Input Low Voltage	V_{IL}	−0.3		0.8	−0.3		0.8	−0.3		0.8	−0.3		0.8	V	
Input High Voltage	V_{IH}	2.4		V_{CC} + 0.3	2.4		V_{CC} + 0.3	2.4		V_{CC} + 0.3	2.4		V_{CC} + 0.3	V	
Output Low Voltage	V_{OL}			0.4			0.4			0.4			0.4	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH}	2.4			2.4			2.4			2.4			V	I_{OH} = −1.0 mA

CAPACITANCE

T_a = 25°C, f = 1 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input/Output Capacitance	$C_{I/O}$			10	pF	$V_{I/O}$ = 0V
Input Capacitance	C_{IN}			5	pF	V_{IN} = 0V

Note: This parameter is periodically sampled and not 100% tested.

AC CHARACTERISTICS

T_a = −40 C to +85 C, V_{CC} = +5V ± 10% unless otherwise noted

PARAMETER	SYMBOL	LIMITS 444/6514-3 MIN	444/6514-3 MAX	444/6514-2 MIN	444/6514-2 MAX	444/6514-1 MIN	444/6514-1 MAX	444/6514 MIN	444/6514 MAX	UNIT	TEST CONDITIONS
READ CYCLE											
Read Cycle	t_{RC}	200		250		300		450		ns	Input Pulse Levels +0.8 to +2.4 Volts
Address Access Time	t_{AA}		200		250		300		450	ns	Input Rise and Fall Times 10 ns
Chip Select Access Time ①	t_{ACS1}		200		250		300		450	ns	Input and Output Timing Levels 1.5 Volt
Chip Select Access Time ②	t_{ACS2}		250		300		350		500	ns	Output Load 1 TTL
Output Hold from Address Change	t_{OH}	50		50		50		50		ns	Gate and C_L = 100 pF
Chip Selection to Output in Low Z	t_{LZ}	20		20		20		20		ns	
Chip Deselection to Output in High Z	t_{HZ}		60		70		80		100	ns	
WRITE CYCLE											
Write Cycle Time	t_{WC}	200		250		300		450		ns	Input Pulse Levels +0.8 to +2.4 Volts
Chip Selection to End of Write	t_{CW}	180		230		250		350		ns	Input Rise and Fall Times 10 ns
Address Valid to End of Write	t_{AW}	180		230		250		350		ns	Input and Output Timing Levels 1.5 Volt
Address Setup Time	t_{AS}	0		0		0		0		ns	Output Load 1 TTL
Write Pulse Width	t_{WP}	180		210		230		300		ns	Gate and C_L = 100 pF
Write Recovery Time	t_{WR}	0		0		0		0		ns	
Data Valid to End of Write	t_{DW}	120		140		150		200		ns	
Data Hold Time	t_{DH}	0		0		0		0		ns	
Write Enabled to Output in High Z	t_{WZ}		60		70		80		100	ns	
Output Active from End of Write	t_{OW}	0		0		0		0		ns	

Notes ① Chip deselected for greater than 100 ns prior to selection

② Chip deselected for a finite time that is less than 100 ns prior to selection. (If the deselect time is 0 ns, the chip is by definition selected and access occurs according to Read Cycle No. 1.)

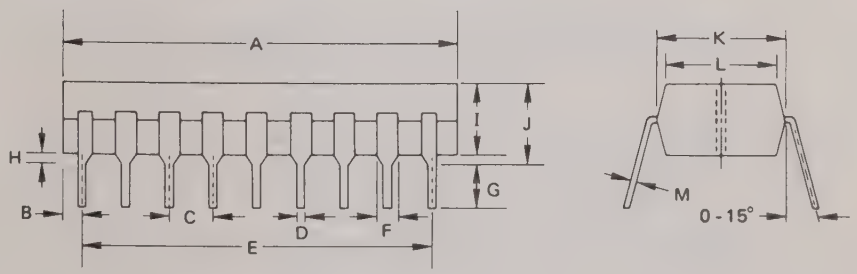
LOW V_{CC} DATA RETENTION CHARACTERISTICS

T_a = −40°C to +85°C

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Data Retention Supply Voltage	V_{CCDR}	2.0			V	$\overline{CS}$ = V_{CC}, V_{IN} = V_{CC} to GND
Data Retention Supply Current	I_{CCDR}		0.1	10	μA	V_{CC} = 3V, $\overline{CS}$ = V_{CC} V_{IN} = V_{CC} to GND
Chip Deselect to Data Retention Time	t_{CDR}	0			ns	
Operation Recovery Time	t_R	t_{RC} ①			ns	

Note: ① t_{RC} = Read Cycle Time

PACKAGE OUTLINE μPD444/6514C

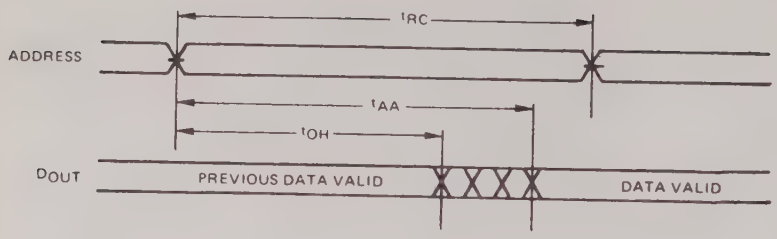


Plastic

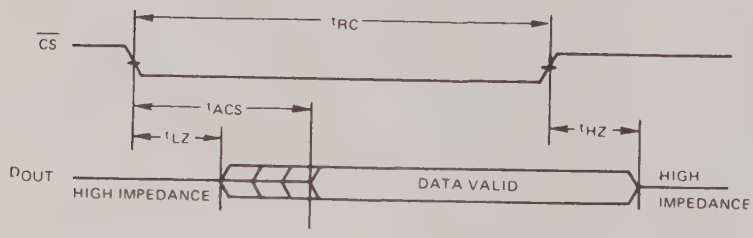
ITEM	MILLIMETERS	INCHES
A	23.2 MAX	0.91 MAX
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.05
G	2.5 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	4.6 MAX.	0.18 MAX
J	5.1 MAX.	0.2 MAX
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

TIMING WAVEFORMS

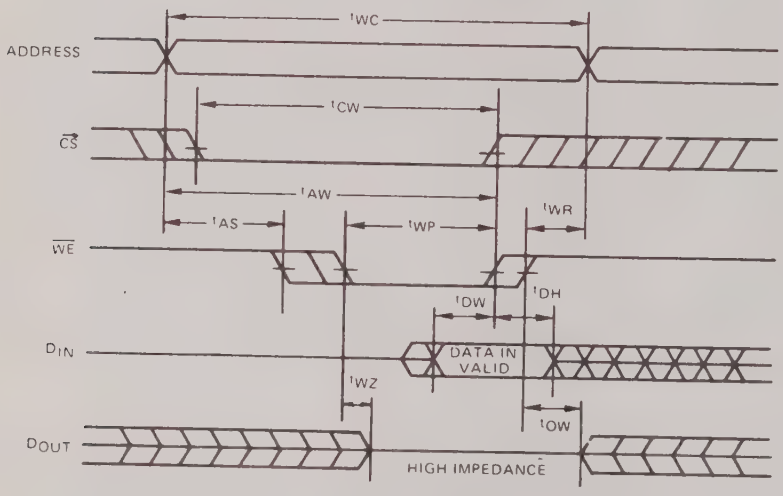
READ CYCLE ① ②



READ CYCLE ① ③

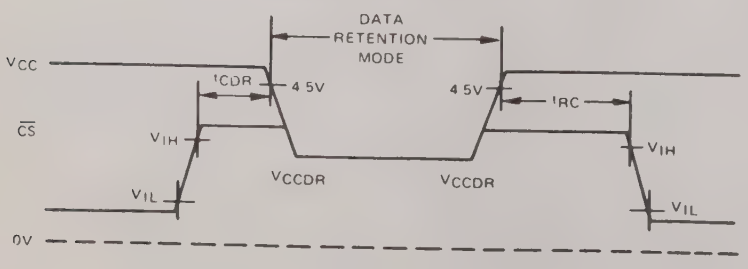


WRITE CYCLE ④ ⑤ ⑥



Notes. ① $\overline{WE}$ is high for Read Cycles.
② Device is continuously selected, $\overline{CS}$ = V_{IL}
③ Address valid prior to or coincident with $\overline{CS}$ transition low.
④ If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition, the output buffers remain in a high impedance state.
⑤ $\overline{WE}$ must be high during all address transitions.
⑥ t_{WP} is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to the earlier of $\overline{CS}$ or $\overline{WE}$ going high.

LOW V_{CC} DATA RETENTION



NEC

NEC Microcomputers

A Division of NEC Electronics U.S.A. Inc.

μPD4016-1/μPD4016-2/μPD4016-3
2048X8 BIT STATIC RAM

Description

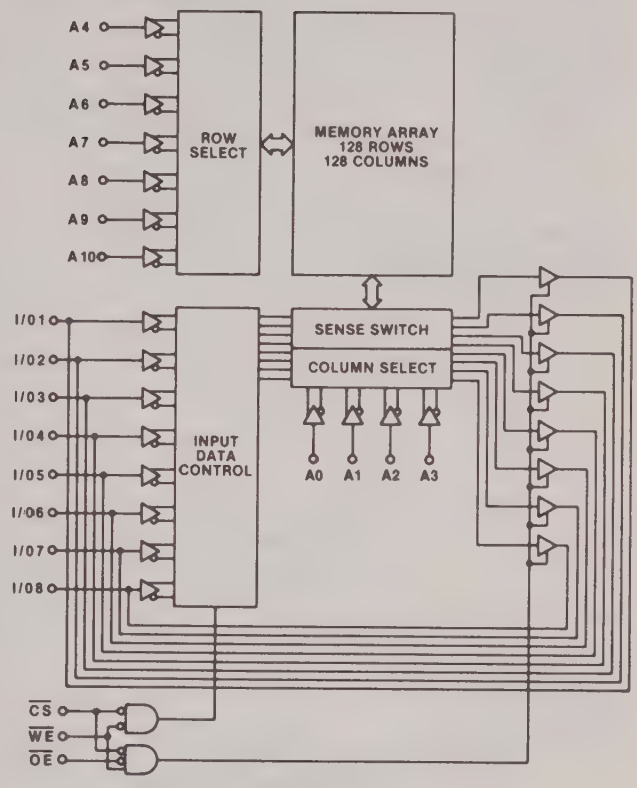
The μPD4016 is a 16384-bit static Random Access Memory device organized as 2048 words by 8 bits. Using a scaled NMOS technology, its design provides the ease-of-use features associated with non-clocked static memories. The μPD4016 has a three-state output and offers a stand-by mode with an attendant 75% savings in power consumption. It features equal access and cycle times and provides an output enable function that eliminates the need for external bus buffers. The μPD4016 is packaged in a standard 24-pin dual-in-line package and is plug-compatible with 16K EPROMS.

Features

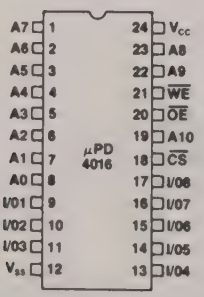
- ☐ Scaled NMOS technology
- ☐ Completely static memory: no clock, no refresh
- ☐ Equal access and cycle times
- ☐ Single +5V supply
- ☐ Automatic power-down
- ☐ All inputs and outputs directly TTL-compatible
- ☐ Common I/O capability
- ☐ $\overline{OE}$ eliminates need for external bus buffers
- ☐ Three-state outputs
- ☐ Plug-compatible with 16K 5V EPROMS
- ☐ Low power dissipation in standby mode
- ☐ Available in a standard 24-pin dual-in-line package

	Access Time	R/W Cycle
μPD4016-1	250 ns	250 ns
μPD4016-2	200 ns	200 ns
μPD4016-3	150 ns	150 ns

Block Diagram



Pin Configuration



Pin Names	
A0 - A10	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/01 - I/08	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground

Truth Table					
$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O	POWER
H	X	X	Not Selected	High-Z	Standby
L	L	H	Read	Dout	Active
L	H	L	Write	Din	Active
L	L	L	Write	Din	Active

Absolute Maximum Ratings

***T_a = 25°C**

Temperature Under Bias	−10°C to 85°C
Storage Temperature	−65°C to 150°C
Voltage on any pin with respect to Ground	−0.5V to 7V
D.C. Output Current	20mA
Power Dissipation	1W

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_a = 25°c, f = 1MHZ

Parameter	Symbol	LIMITS Min.	Typ.	Max.	Unit	Test Conditions
Input Capacitance	C_{IN}			5	pF	V_{IN} = 0V
I/O Capacitance	$C_{I/O}$			7	pF	$V_{I/O}$ = 0V
This parameter is sampled and not 100% tested.						

DC Characteristics

T_a = 0°c to 70°c, V_{CC} 5V ± 10%

Parameter	Symbol	LIMITS Min.	Typ.	Max.	Unit	Test Conditions
Input Leakage Current	I_{LI}			10	μA	VCC = Max. VIN = GND to VCC
Output Leakage Current	I_{LO}			10	μA	VCC = Max. $\overline{CS}$ = VIH VOUT = GND to VCC
Operating Current	I_{CC}			60	mA	VCC = Max. $\overline{CS}$ = VIL Outputs Open
Standby Current	I_{SB}			15	mA	VCC = Min. to Max. $\overline{CS}$ = VIH
Input Low Voltage	V_{IL}	0.3		0.8	V	
Input High Voltage	V_{IH}	2.0		6.0	V	
Output Low Voltage	V_{OL}			0.4	V	IOL = 4mA
Output High Voltage	V_{OH}	2.4			V	IOH = −1mA
Output Short Circuit Current	I_{OS}	TBD		TBD	mA	VOUT = GND to VCC

AC Test Conditions

Input Pulse Levels ..... 0.8V to 2.2V
Input Rise and Fall Times 10nsec
Input Timing Reference Levels 1.5V
Output Timing Reference Levels 1.5V

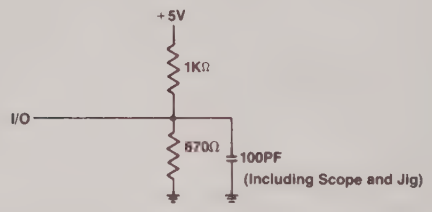


Figure 1 – Output Load

AC Characteristics

Read Cycle

T_a = 0°c to 70°c, V_{CC} 5V ± 10%

Parameter	Symbol	LIMITS μPD4016-3 Min.	μPD4016-3 Max.	μPD4016-2 Min.	μPD4016-2 Max.	μPD4016-1 Min.	μPD4016-1 Max.	Unit	Notes
Read Cycle Time	t_{RC}	150		200		250		nsec	1
Address Access Time	t_{AA}		150		200		250	nsec	
Chip Select Access Time	t_{ACS}		150		200		250	nsec	2
Output Hold from Address Change	t_{OH}	10		10		10		nsec	
Chip Selection to Output in Low Z	t_{LZ}	10		10		10		nsec	3,4
Chip Deselection to Output in High Z	t_{HZ}		50		60		80	nsec	3,4
Output Enable to Output Valid	t_{OE}		70		90		110	nsec	
Output Enable to Output in Low Z	t_{OLZ}	10		10		10		nsec	3,4
Output Disable to Output in High Z	t_{OHZ}		50		60		80	nsec	3,4
Chip Selection to Power up Time	t_{PU}	0		0		0		nsec	4
Chip Deselection to Power down Time	t_{PD}		70		90		110	nsec	4

Write Cycle

T_a = 0°c to 70°c, V_{CC} 5V ± 10%

Parameter	Symbol	LIMITS μPD4016-3 Min.	μPD4016-3 Max.	μPD4016-2 Min.	μPD4016-2 Max.	μPD4016-1 Min.	μPD4016-1 Max.	Unit	Notes
Write Cycle Time	t_{WC}	150		200		250		nsec	
Chip Selection to End of Write	t_{CW}	120		160		200		nsec	
Address Valid to End of Write	t_{AW}	90		120		150		nsec	
Address Setup Time	t_{AS}	0		0		0		nsec	
Write Pulse Width	t_{WP}	80		100		130		nsec	5
Write Recovery Time	t_{WR}	10		10		10		nsec	
Data Valid to End of Write	t_{DW}	50		60		80		nsec	
Data Hold Time	t_{DH}	0		0		0		nsec	
Write Enabled to Output in High-Z	t_{WZ}		50		60		80	nsec	6,7
Output Active from End of Write	t_{OW}	10		10		10		nsec	6,7

Notes:

1. All Read Cycle timings are referenced from the last valid address to the first transitioning address.
2. Address valid prior to or coincident with $\overline{CS}$ transition low.
3. Transition is measured ± 200mV from steady state voltage with specified load of Figure 1.
4. This parameter is sampled and not 100% tested.
5. If $\overline{CS}$ and $\overline{OE}$ are both low before write enabled, tWP = tWZ + DW
6. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2.
7. This parameter is sampled and not 100% tested.

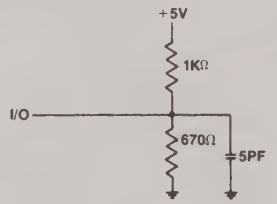
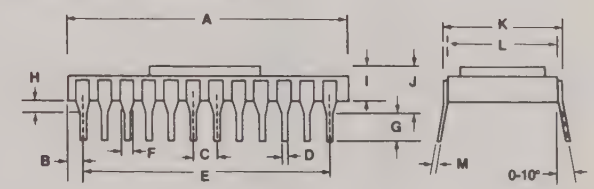


Figure 2 - Transition Load

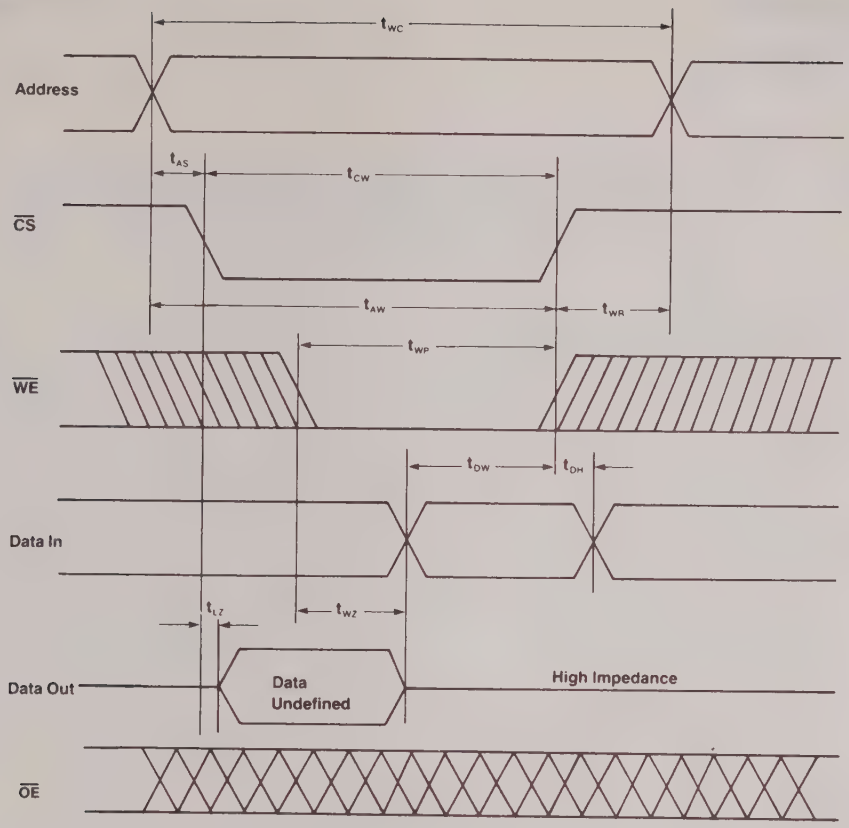
Package Outline μPD4016D (Ceramic)



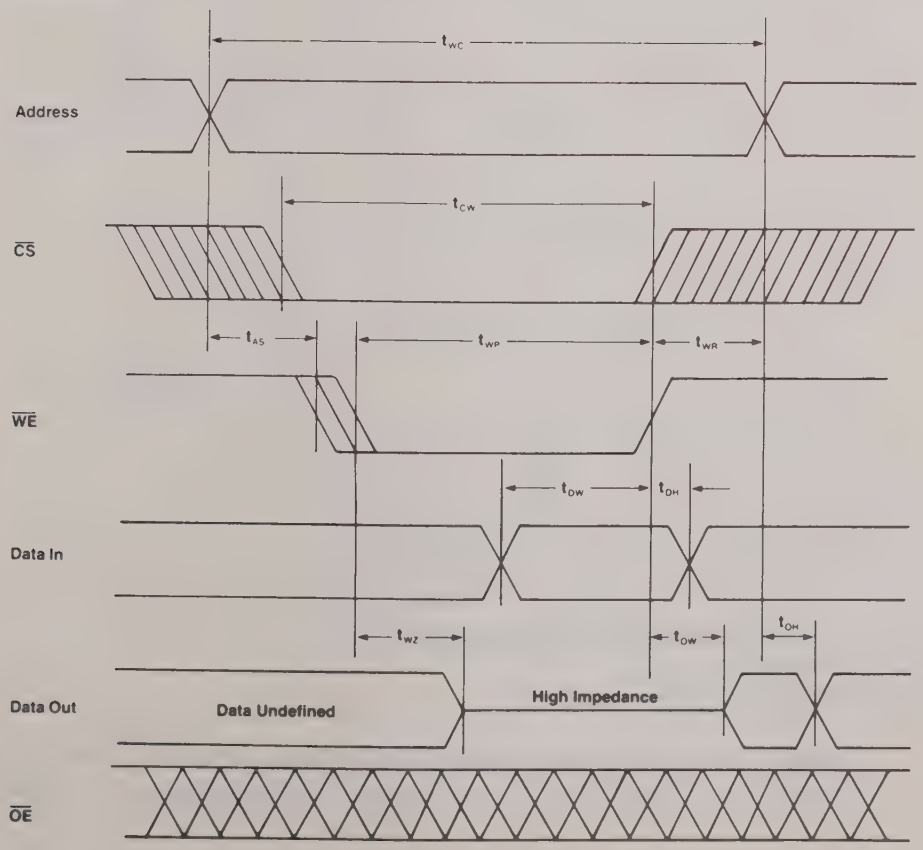
Item	Millimeters	Inches
A	30.78 MAX.	1.23 MAX.
B	1.53 MAX.	0.07 MAX.
C	2.54 ± 0.1	0.10 ± 0.004
D	0.46 ± 0.8	0.018 ± 0.03
E	27.94 ± 0.1	1.10 ± 0.004
F	1.02 MIN.	0.04 MIN.
G	3.2 MIN.	0.125 MIN.
H	1.02 MIN.	0.04 MIN.
I	3.23 MAX.	0.13 MAX.
J	4.25 MAX.	0.17 MAX.
K	15.24 TYP.	0.60 TYP.
L	14.93 TYP.	0.59 TYP.
M	0.25 ± 0.05	0.010 ± 0.002

Timing Waveforms

Write Cycle No. 1 ($\overline{WE}$ Controlled)



Write Cycle No. 2 ($\overline{CS}$ Controlled)



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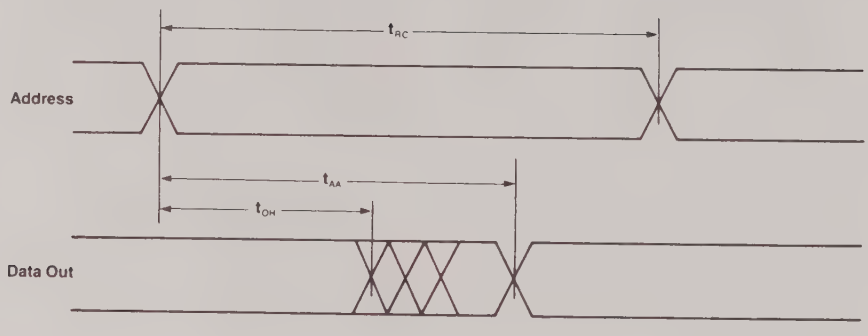
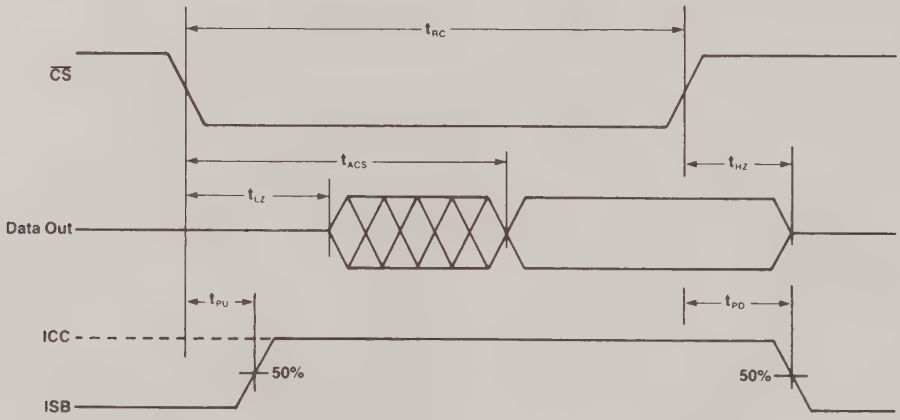
NEC Microcomputers
A Division of NEC Electronics U.S.A. Inc.

173 Worcester Street
Wellesley, Massachusetts 02181
Tel: 617-237-1910
TWX: 710-383-1745

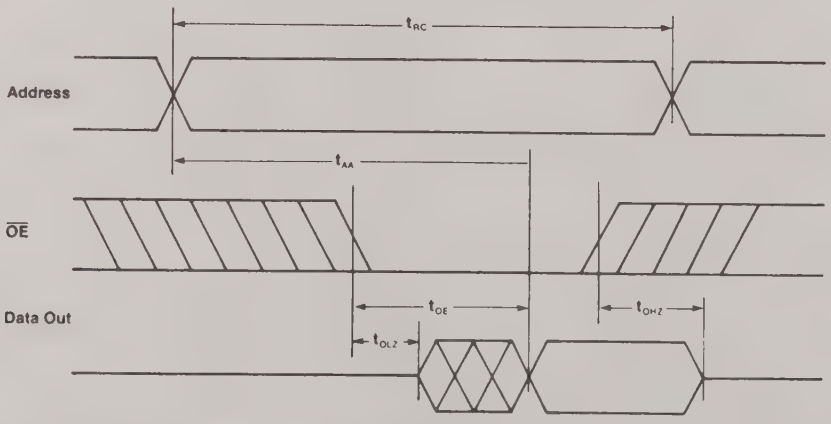
Read Cycle No. 1 ② ③ ④



Read Cycle No. 2 ① ② ④



Read Cycle No. 3 ② ③



Notes: ① Address valid prior to or coincident with $\overline{CS}$ transition low.
② $\overline{WE}$ is high for Read Cycles.
③ Device is continuously selected, $\overline{CS}$ = VIL.
④ $\overline{OE}$ = VIL

The information presented in this document is believed to be accurate and reliable. It is subject to change without notice.

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4016-5-81-4K

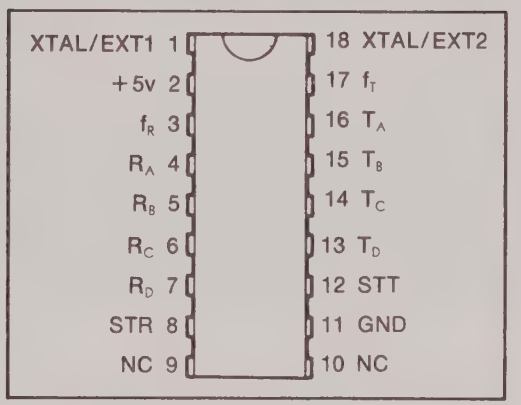
COM 8116
COM 8116T

Dual Baud Rate Generator
Programmable Divider

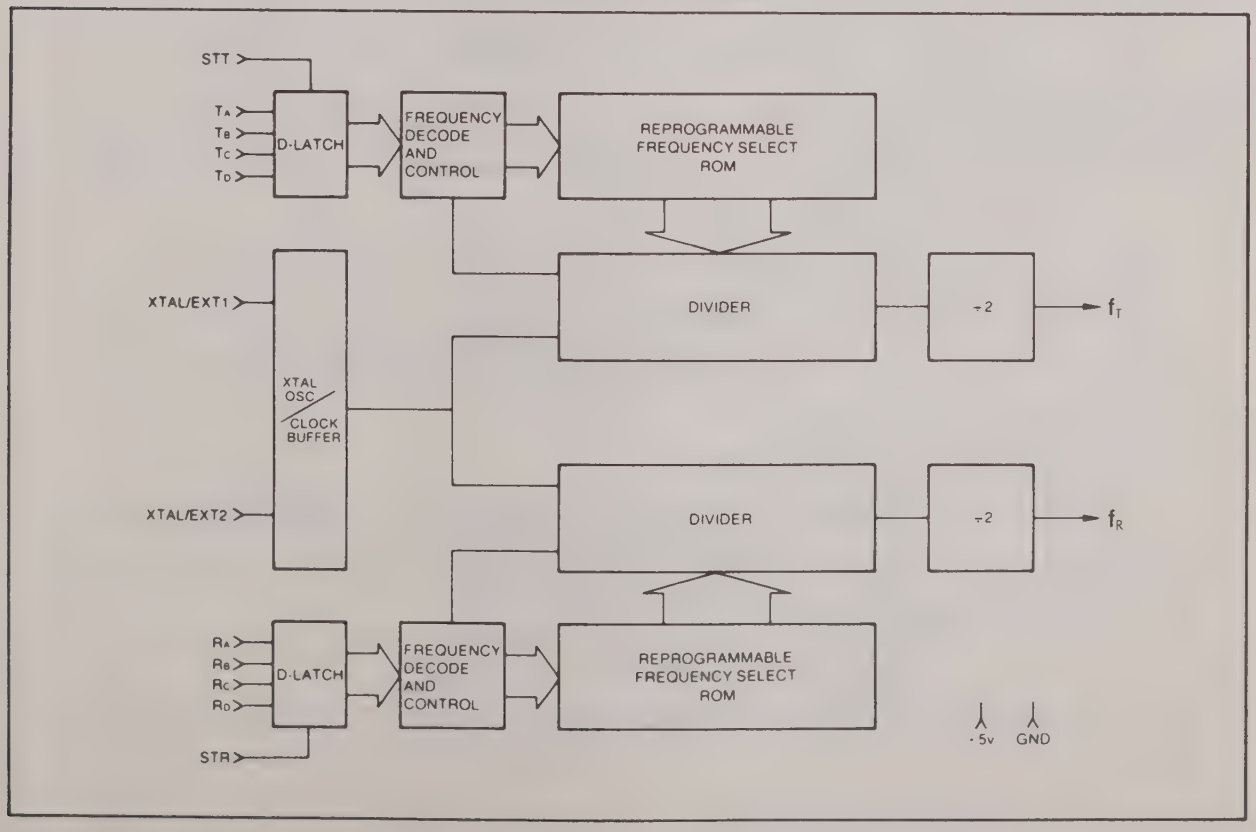
FEATURES

- ☐ On chip crystal oscillator or external frequency input
- ☐ Single +5v power supply
- ☐ Choice of 2 x 16 output frequencies
- ☐ 16 asynchronous/synchronous baud rates
- ☐ Direct UART/USRT/ASTRO/USYNRT compatibility
- ☐ Full duplex communication capability
- ☐ Re-programmable ROM via CLASP™ technology allows generation of other frequencies
- ☐ TTL, MOS compatibility
- ☐ Compatible with COM 5016

PIN CONFIGURATION



BLOCK DIAGRAM



General Description

The Standard Microsystem's COM 8116 is an enhanced version of the COM 5016 Dual Baud Rate Generator. It is fabricated using SMC's patented COPLAMOS® and CLASP™ technologies and employs depletion mode loads, allowing operation from a single +5v supply.

The standard COM 8116 is specifically dedicated to generating the full spectrum of 16 asynchronous/synchronous data communication frequencies for 16X UART/USRT devices. A large number of the frequencies available are also useful for 1X and 32X ASTRO/USYNRT devices.

The COM 8116 features an internal crystal oscillator which may be used to provide the master reference frequency. Alternatively, an external reference may be supplied by applying complementary TTL level signals to pins 1 and 18. Parts suitable for use only with an external TTL reference are marked COM 8116T. TTL outputs used to drive the COM 8116 or COM 8116T XTAL/EXT inputs should not be used to drive other TTL inputs, as noise immunity may be compromised due to excessive loading.

The output of the oscillator/buffer is applied to the dividers for generation of the output frequencies f_T, f_R. The dividers are capable of dividing by any integer from 6 to $2^{19} + 1$, inclusive. If the divisor is even, the output will be square; otherwise the output will be high longer than it is low by one fx clock period.

Each of the two divisor ROMs contains 16 divisors, each 19 bits wide, and is fabricated using SMC's unique CLASP™ technology allowing up to 32 different divisors on custom parts. This process permits reduction of turn-around time for ROM patterns. Each group of four divisor select bits is held in an externally strobed data latch. The strobe input is level sensitive: while the strobe is high, data is passed directly through to the ROM. Initiation of a new frequency is effected within 3.5μs of a change in any of the four divisor select bits (strobe activity is not required). The divisor select inputs have pull-up resistors; the strobe inputs do not.

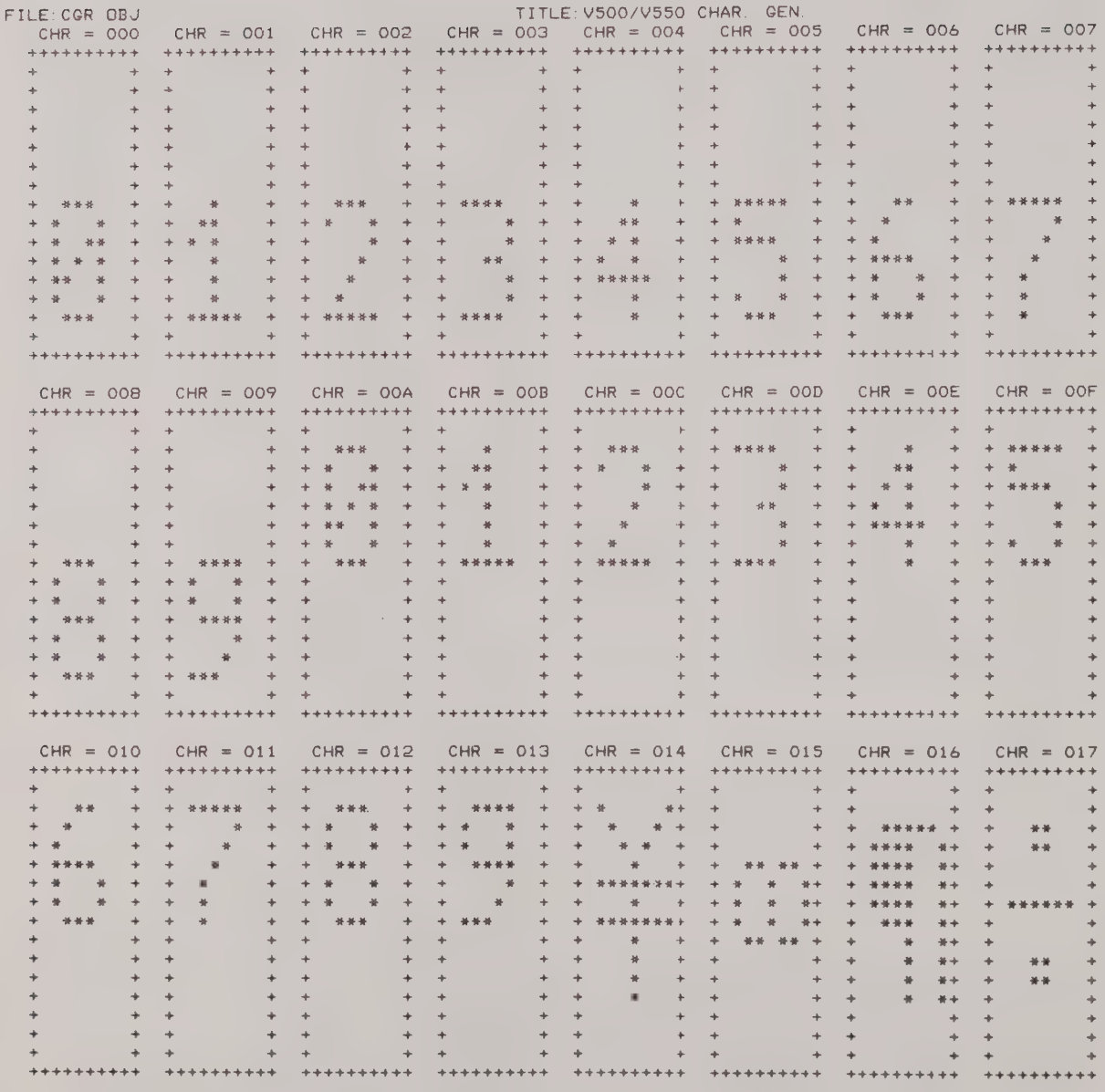
Description of Pin Functions

Pin No.	Symbol	Name	Function
1	XTAL/EXT1	Crystal or External Input 1	This input is either one pin of the crystal package or one polarity of the external input.
2	V_{CC}	Power Supply	+5 volt supply
3	f_R	Receiver Output Frequency	This output runs at a frequency selected by the Receiver divisor select data bits.
4-7	R_A, R_B, R_C, R_D	Receiver-Divisor Select Data Bits	The logic level on these inputs, as shown in Table 1, selects the receiver output frequency, f_R.
8	STR	Strobe-Receiver	A high level input strobe loads the receiver data (R_A, R_B, R_C, R_D) into the receiver divisor select register. This input may be strobed or hard-wired to a high level.
9	NC	No Connection	
10	NC	No Connection	
11	GND	Ground	Ground
12	STT	Strobe-Transmitter	A high level input strobe loads the transmitter data (T_A, T_B, T_C, T_D) into the transmitter divisor select register. This input may be strobed or hard-wired to a high level.
13-16	T_D, T_C, T_B, T_A	Transmitter-Divisor Select Data Bits	The logic level on these inputs, as shown in Table 1, selects the transmitter output frequency, f_T.
17	f_T	Transmitter Output Frequency	This output runs at a frequency selected by the Transmitter divisor select data bits.
18	XTAL/EXT2	Crystal or External Input 2	This input is either the other pin of the crystal package or the other polarity of the external input.

COM 8116T-020
Reference Frequency = 1.8432 MHz

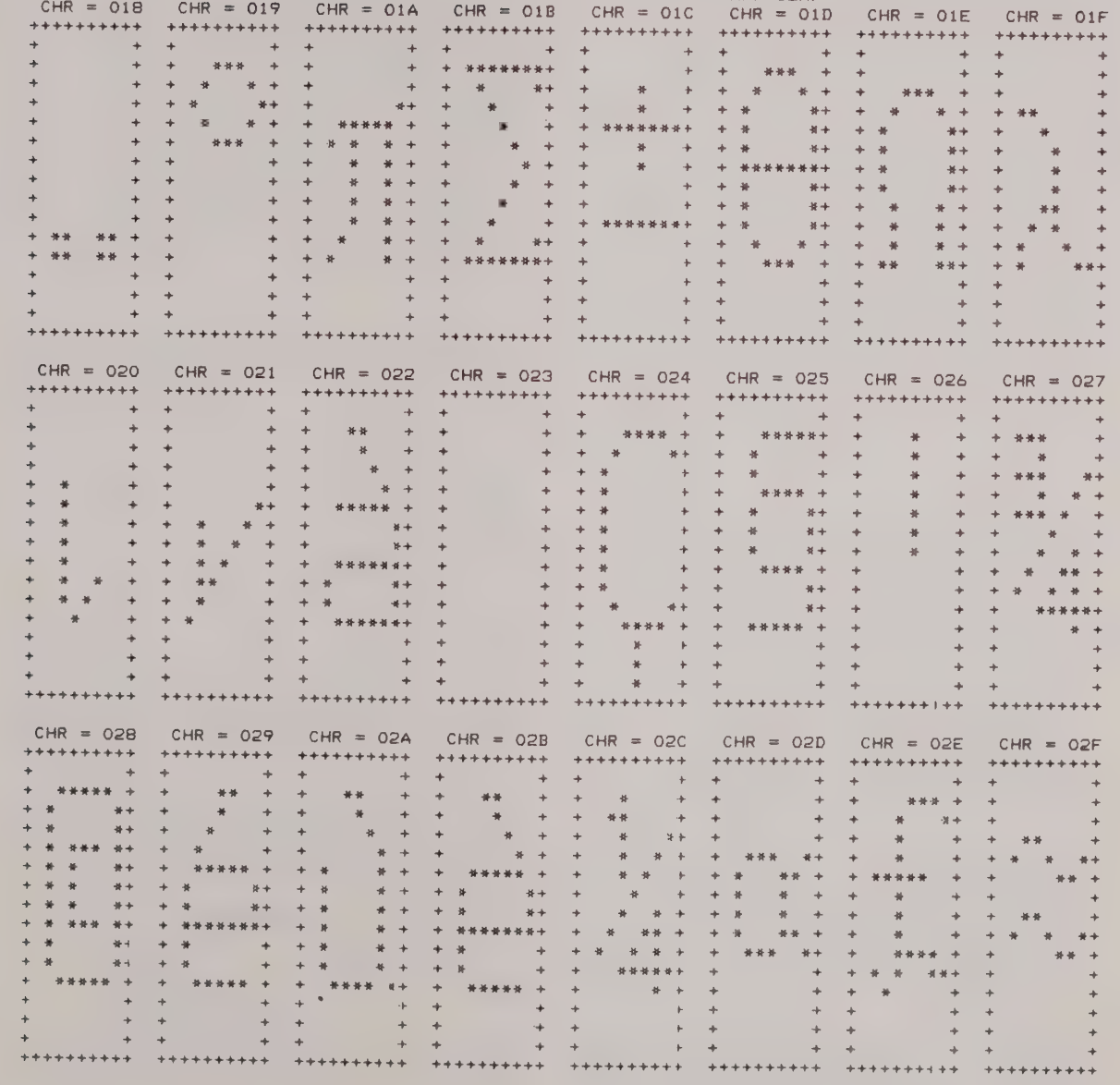
Divisor Select DCBA	Desired Baud Rate	Clock Factor	Desired Frequency (KHz)	Divisor	Actual Baud Rate	Actual Frequency (KHz)	Deviation
0000	50.00	16X	0.80000	2304	50.00	0.800000	0.0000%
0001	75.00	16X	1.20000	1536	75.00	1.200000	0.0000%
0010	110.00	16X	1.76000	1047	110.00	1.761000	0.0000%
0011	134.50	16X	2.15200	856	134.52	2.151	0.0000%
0100	150.00	16X	2.40000	768	150.00	2.400000	0.0000%
0101	200.00	16X	3.20000	576	200.00	3.200000	0.0000%
0110	300.00	16X	4.80000	384	300.00	4.800000	0.0000%
0111	600.00	16X	9.60000	192	600.00	9.600000	0.0000%
1000	1200.00	16X	19.20000	96	1200.00	19.200000	0.0000%
1001	1800.00	16X	28.80000	64	1800.00	28.801000	0.0000%
1010	2000.00	16X	32.20000	57	1986.00	31.780	1.3 %
1011	2400.00	16X	38.40000	48	2400.00	38.402000	0.0000%
1100	3600.00	16X	57.60000	32	3600.00	57.602000	0.0000%
1101	4800.00	16X	76.80000	24	4800.00	76.803000	0.0000%
1110	9600.00	16X	153.60000	12	9600.00	153.607000	0.0000%
1111	19200.00	16X	307.20000	6	19200.00	307.213	0.0000%

MATH SYMBOL SET #1



DATE: JUN-28-1982 16:11:15

FILE: CGR.OBJ TITLE: V500/V550 CHAR. GEN.



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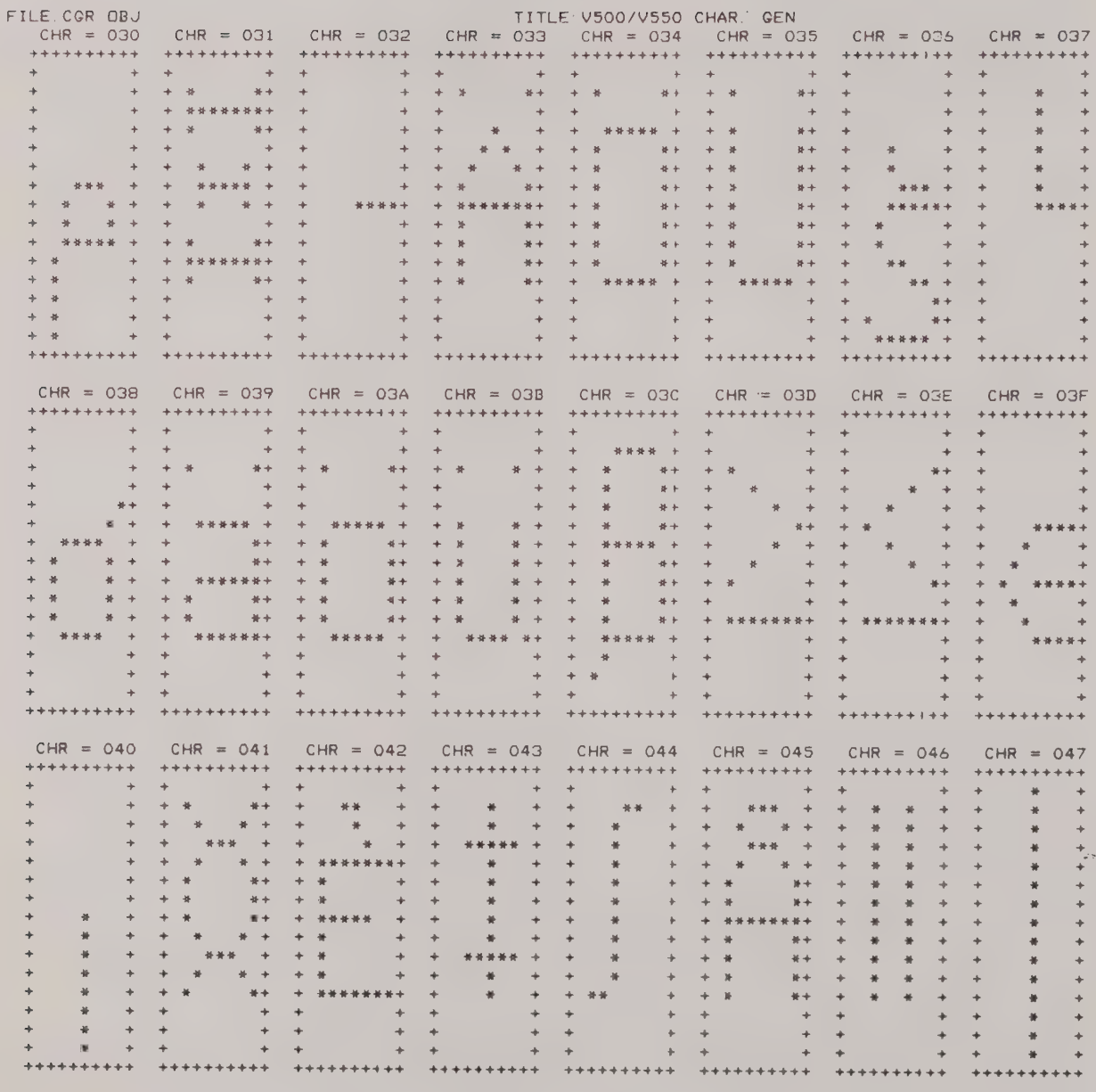


NEC

NEC Microcomputers

A Division of NEC Electronics U.S.A. Inc.

μPD7220/GDC GRAPHICS DISPLAY CONTROLLER

PRELIMINARY

Description

The μPD7220 Graphics Display Controller (GDC) is an intelligent microprocessor peripheral designed to be the heart of a high-performance raster-scan computer graphics and character display system. Positioned between the video display memory and the microprocessor bus, the GDC performs the tasks needed to generate the raster display and manage the display memory. Processor software overhead is minimized by the GDC's sophisticated instruction set, graphics figure drawing, and DMA transfer capabilities. The display memory supported by the GDC can be configured in any number of formats and sizes up to 256K 16-bit words. The display can be zoomed and panned, while partitioned screen areas can be independently scrolled. With its light pen input and multiple controller capability, the GDC is ideal for advanced computer graphics applications.

Features

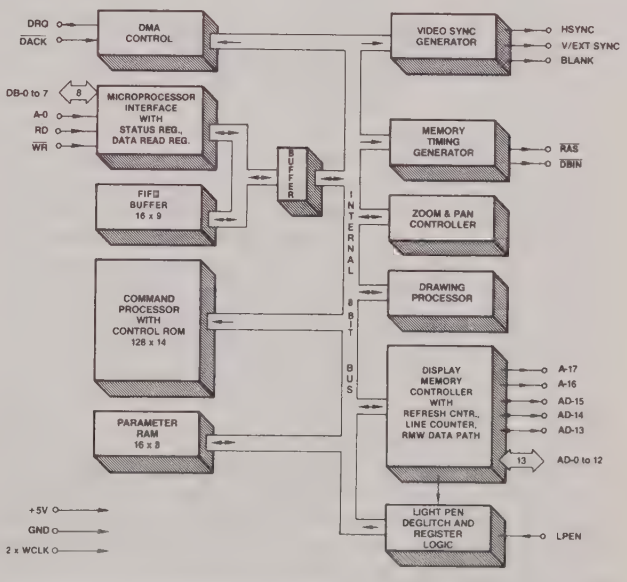
- ☐ Microprocessor Interface
  - DMA transfers with 8257 or 8237-type controllers
  - FIFO Command Buffering
- ☐ Display Memory Interface
  - Up to 256K words of 16 bits
  - Read-Modify-Write (RMW) Display Memory cycles in under 800ns
  - Dynamic RAM refresh cycles for non-accessed memory
- ☐ Light Pen Input
- ☐ External video synchronization mode
- ☐ Graphics Mode:
  - Four megabit, bit-mapped display memory
- ☐ Character Mode:
  - 8K character code and attributes display memory
- ☐ Mixed Graphics and Characters Mode
  - 64K if all characters
  - 1 megapixel if all graphics
- ☐ Graphics Capabilities:
  - Figure drawing of lines, arc/circles, rectangles, and graphics character in 800ns per pixel
  - Display 1024 by 1024 pixels with 4 planes of color or grayscale
  - Two independently scrollable areas
- ☐ Character Capabilities:
  - Auto cursor advance
  - Four independently scrollable areas
  - Programmable cursor height
  - Characters per row: up to 256
  - Character rows per screen: up to 100
- ☐ Video Display Format
  - Zoom magnification factors of 1 to 16
  - Panning
  - Command-settable video raster parameters
- ☐ Technology
  - Single +5 volt, NMOS, 40-pin DIP
- ☐ DMA Capability:
  - Bytes or word transfers
  - 4 clock periods per byte transferred

System Considerations

The GDC is designed to work with a general purpose microprocessor to implement a high-performance computer graphics system. Through the division of labor established by the GDC's design, each of the system components is used to the maximum extent through six-level hierarchy of simultaneous tasks. At the lowest level, the GDC generates the basic video raster timing, including sync and blanking signals. Partitioned areas on the screen and zooming are also accomplished at this level. At the next level, video display memory is modified during the figure drawing operations and data moves. Third, display memory addresses are calculated pixel by pixel as drawing progresses. Outside the GDC at the next level, preliminary calculations are done to prepare drawing parameters. At the fifth level, the picture must be represented as a list of graphics figures drawable by the GDC. Finally, this representation must be manipulated, stored, and communicated. By handling the first three levels, the GDC takes care of the high-speed and repetitive tasks required to implement a graphics system.

GDC Components

The GDC block diagram illustrates how these tasks are accomplished.



Microprocessor Bus Interface

Control of the GDC by the system microprocessor is achieved through an 8-bit bi-directional interface. The status register is readable at any time. Access to the FIFO buffer is coordinated through flags in the status register and operates independently of the various internal GDC operations, due to the separate data bus connecting the interface and the FIFO buffer.

Command Processor

The contents of the FIFO are interpreted by the command processor. The command bytes are decoded, and the succeeding parameters are distributed to their proper destina-

tions within the GDC. The command processor yields to the bus interface when both access the FIFO simultaneously.

DMA Control
The DMA control circuitry in the GDC coordinates transfers over the microprocessor interface when using an external DMA controller. The DMA Request and Acknowledge handshake lines directly interface with a μPD8257 or μPD8237 DMA controller, so that display data can be moved between the microprocessor memory and the display memory.

Parameter RAM
The 16-byte RAM stores parameters that are used repetitively during the display and drawing processes. In character mode, this RAM holds four sets of partitioned display area parameters; in graphics mode, the drawing pattern and graphics character take the place of two of the sets of parameters.

Video Sync Generator
Based on the clock input, the sync logic generates the raster timing signals for almost any interlaced, non-interlaced, or "repeat field" interlaced video format. The generator is programmed during the idle period following a reset. In video sync slave mode, it coordinates timing between multiple GDCs.

Memory Timing Generator
The memory timing circuitry provides two memory cycle types: a two-clock period refresh cycle and the read-modify-write (RMW) cycle which takes four clock periods. The memory control signals needed to drive the display memory devices are easily generated from the GDC's RAS and DBIN outputs.

Zoom & Pan Controller
Based on the programmable zoom display factor and the display area entries in the parameter RAM, the zoom and pan controller determines when to advance to the next memory address for display refresh and when to go on to the next display area. A horizontal zoom is produced by slowing down the display refresh rate while maintaining the video sync rates. Vertical zoom is accomplished by repeatedly accessing each line a number of times equal to the horizontal repeat. Once the line count for a display area is exhausted, the controller accesses the starting address and line count of the next display area from the parameter RAM. The system microprocessor, by modifying a display area starting address, can pan in any direction, independent of the other display areas.

Drawing Processor
The drawing processor contains the logic necessary to calculate the addresses and positions of the pixels of the various graphics figures. Given a starting point and the appropriate drawing parameters, the drawing processor needs no further assistance to complete the figure drawing.

Display Memory Controller
The display memory controller's tasks are numerous. Its primary purpose is to multiplex the address and data information in and out of the display memory. It also contains the 16-bit logic unit used to modify the display memory contents during RMW cycles, the character mode line counter, and the refresh counter for dynamic RAMs. The memory controller apportions the video field time between the various types of cycles.

Light Pen Deglitcher
Only if two rising edges on the light pen input occur at the same point during successive video fields are the pulses accepted as a valid light pen detection. A status bit indicates to the system microprocessor that the light pen register contains a valid address.

Programmer's View of GDC
The GDC occupies two addresses on the system microprocessor bus through which the GDC's status register and FIFO are accessed. Commands and parameters are written into the GDC's FIFO and are differentiated based on address bit A0. The status register or the FIFO can be read as selected by the address line.

A0	READ	WRITE
0	STATUS REGISTER	PARAMETER INTO FIFO
1	FIFO READ	COMMAND INTO FIFO

GDC Microprocessor Bus Interface Registers

Commands to the GDC take the form of a command byte followed by a series of parameter bytes as needed for specifying the details of the command. The command processor decodes the commands, unpacts the parameters, loads them into the appropriate registers within the GDC, and initiates the required operations.

The commands available in the GDC can be organized into five categories as described in the following section.

GDC Command Summary

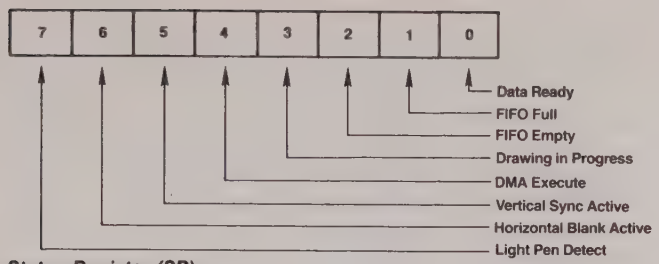
Video Control Commands
1. RESET: Resets the GDC to its idle state and specifies the video display format.
2. VSYNC: Selects master or slave video synchronization mode.
3. CCHAR: Specifies the cursor and character row heights.

Display Control Commands
1. START: Starts the display scanning process.
2. ZOOM: Specifies zoom factors for the display and graphics characters writing.
3. CURS: Sets the position of the cursor in display memory.
4. PRAM: Defines starting addresses and lengths of the display areas and specifies the eight bytes for the graphics character.
5. PITCH: Specifies the width of the X dimension of display memory.

Drawing Control Commands
1. WDAT: Writes data words or bytes into display memory.
2. MASK: Sets the mask register contents.
3. FIGS: Specifies the parameters for the drawing processor.
4. FIGD: Draws the figure as specified above.
5. GCHRD: Draws the graphics character into display memory.

Data Read Commands
1. RDAT: Reads data words or bytes from display memory.
2. CURD: Reads the cursor position.
3. LPRD: Reads the light pen address.

DMA Control Commands
1. DMAR: Requests a DMA read transfer.
2. DMAW: Requests a DMA write transfer.



Status Register (SR)

Status Register Flags

SR-7: Light Pen Detect
When this bit is set to 1, the light pen address (LAD) register contains a deglitched value that the system microprocessor may read. This flag is reset after the 3-byte LAD is moved into the FIFO in response to the light pen read command.

SR-6: Horizontal Blanking Active
A 1 value for this flag signifies that horizontal retrace blanking is currently underway.

SR-5: Vertical Sync
Vertical retrace sync occurs while this flag is a 1. The vertical sync flag coordinates display format modifying commands to the blanked interval surrounding vertical sync. This eliminates display disturbances.

SR-4: DMA Execute
This bit is a 1 during DMA data transfers.

SR-3: Drawing in Progress
While the GDC is drawing a graphics figure, this status bit is a 1.

SR-2: FIFO Empty
This bit and the FIFO Full flag coordinate system microprocessor accesses with the GDC FIFO. When it is 1, the Empty flag ensures that all the commands and parameters previously sent to the GDC have been processed.

SR-1: FIFO Full
A 1 at this flag indicates a full FIFO in the GDC. A 0 ensures that there is room for at least one byte. This flag needs to be checked before each write into the GDC.

SR-0: Data Ready
When this flag is a 1, it indicates that a byte is available to be read by the system microprocessor. This bit must be tested before each read operation. It drops to a 0 while the data is transferred from the FIFO into the microprocessor interface data register.

FIFO Operation & Command Protocol

The first-in, first-out buffer (FIFO) in the GDC handles the command dialogue with the system microprocessor. This flow of information uses a half-duplex technique, in which the single 16-location FIFO is used for both directions of data movement, one direction at a time. The FIFO's direction is controlled by the system microprocessor through the GDC's command set. The microprocessor coordinates these transfers by checking the appropriate status register bits.

The command protocol used by the GDC requires the differentiation of the first byte of a command sequence from the succeeding bytes. This first byte contains the operation code and the remaining bytes carry parameters. Writing into the GDC causes the FIFO to store a flag value alongside the data byte to signify whether the byte was written into the command or the parameter address. The command processor in the GDC tests this bit as it interprets the entries in the FIFO.

The receipt of a command byte by the command processor marks the end of any previous operation. The number of parameter bytes supplied with a command is cut short by the receipt of the next command byte. A read operation from the GDC to the microprocessor can be terminated at any time by the next command.

The FIFO changes direction under the control of the system microprocessor. Commands written into the GDC always put the FIFO into write mode if it wasn't in it already. If it was in read mode, any read data in the FIFO at the time of the turnaround is lost. Commands which require a GDC response, such as RDAT CURD and LPRD, put the FIFO into read mode after the command is interpreted by the GDC's command processor. Any commands and parameters behind the read-evoking command are discarded when the FIFO direction is reversed.

Read-Modify-Write Cycle

Data transfers between the GDC and the display memory are accomplished using a read-modify-write (RMW) memory cycle. The four clock period timing of the RMW cycle is used to: 1) output the address, 2) read data from the memory, 3) modify the data, and 4) write the modified data back into the initially selected memory address. This type of memory cycle is used for all interactions with display memory including DMA transfers, except for the two clock period display and RAM refresh cycles.

The operations performed during the modify portion of the RMW cycle merit additional explanation. The circuitry in the GDC uses three main elements: the Pattern register, the Mask register, and the 16-bit Logic Unit. The Pattern register holds the data pattern to be moved into memory. It is loaded by the WDAT command or, during drawing, from the parameter RAM. The Mask register contents determine which bits of the read data will be modified. Based on the contents of these registers, the Logic Unit performs the selected operations of REPLACE, COMPLEMENT, SET, or CLEAR on the data read from display memory.

The Pattern register contents are ANDed with the Mask register contents to enable the actual modification of the memory read data, on a bit-by-bit basis. For graphics drawing, one bit at a time from the Pattern register is combined with the Mask. When ANDed with the bit set to a 1 in the Mask register, the proper single pixel is modified by the Logic Unit. For the next pixel in the figure, the next bit in the Pattern register is selected and the Mask register bit is moved to identify the pixel's location within the word. The Execution word address pointer register, EAD, is also adjusted as required to address the word containing the next pixel.

In character mode, all of the bits in the Pattern register are used in parallel to form the respective bits of the modify data word. Since the bits of the character code word are used in parallel, unlike the one-bit-at-a-time graphics drawing process, this facility allows any or all of the bits in a memory word to be modified in one RMW memory cycle. The Mask register must be loaded with 1s in the positions where modification is to be permitted.

The Mask register can be loaded in either of two ways. In graphics mode, the CURS command contains a four-bit dAD field to specify the dot address. The command processor converts this parameter into the one-of-16 format used in the Mask register for figure drawing. A full 16 bits can be loaded into the Mask register using the MASK command. In addition to the character mode use mentioned above, the 16-bit MASK load is convenient in graphics mode when all of the pixels of a word are to be set to the same value.

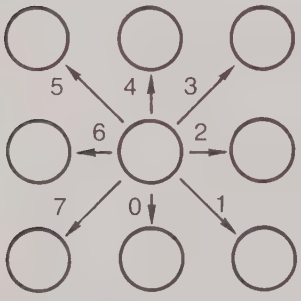
The Logic Unit combines the data read from display memory, the Pattern Register, and the Mask register to generate the data to be written back into display memory. Any one of four operations can be selected: REPLACE, COMPLEMENT, CLEAR or SET. In each case, if the respective Mask bit is 0, that particular bit of the read data is returned to memory unmodified. If the Mask bit is 1, the modification is enabled. With the REPLACE operation, the modify data simply takes the place of the read data for modification enabled bits. For the other three operations, a 0 in the modify data allows the read data bit to be returned to memory. A 1 value causes the specified operation to be performed in the bit positions with set Mask bits.

Figure Drawing

The GDC draws graphics figures at the rate of one pixel per read-modify-write (RMW) display memory cycle. These cycles take four clock periods to complete. At a clock frequency of 5MHZ, this is equal to 800ns. During the RMW cycle the GDC simultaneously calculates the address and position of the next pixel to be drawn.

The graphics figure drawing process depends on the display memory addressing structure. Groups of 16 horizontally adjacent pixels form the 16-bit words which are handled by the GDC. Display memory is organized as a linearly addressed space of these words. Addressing of individual pixels is handled by the GDC's internal RMW logic.

During the drawing process, the GDC finds the next pixel of the figure which is one of the eight nearest neighbors of the last pixel drawn. The GDC assigns each of these eight directions a number from 0 to 7, starting with straight down and proceeding counterclockwise.



Drawing Directions

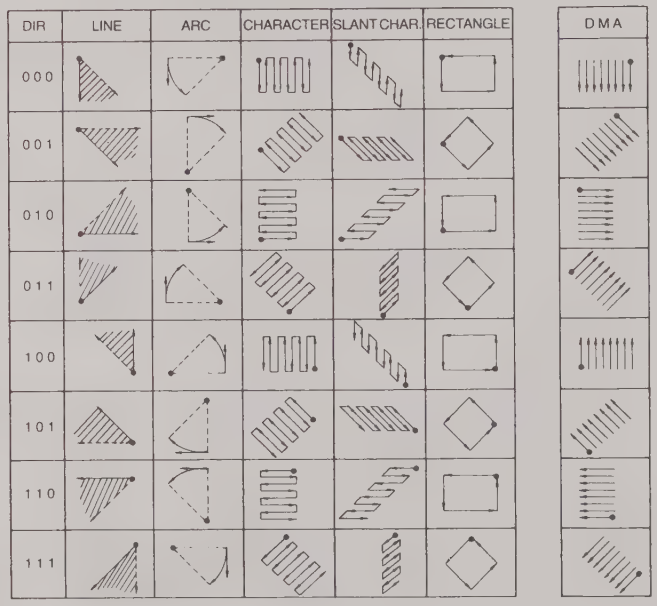
Figure drawing requires the proper manipulation of the address and the pixel bit position according to the drawing direction to determine the next pixel of the figure. To move to the word above or below the current one, it is necessary to subtract or add the number of words per line in display memory. This parameter is called the pitch. To move to the word to either side, the Execute word address cursor, EAD, must be incremented or decremented as the dot address pointer bit reaches the LSB or the MSB of the Mask register. To move to a pixel within the same word, it is necessary to rotate the dot address pointer register to the right or left. The table below summarizes these operations for each direction.

Whole word drawing is useful for filling areas in memory with a single value. By setting the Mask register to all 1s with the MASK command, both the LSB and MSB of the dAD will always be 1, so that the EAD value will be incremented or decremented for each cycle regardless of direction. One RMW cycle will be able to effect all 16 bits of the word for any drawing type. One bit in the Pattern register is used per RMW cycle to write all the bits of the word to the same value. The next Pattern bit is used for the word, etc.

DIR	OPERATIONS TO ADDRESS THE NEXT PIXEL
000	EAD + P → EAD
001	EAD + P → EAD dAD (MSB) = 1 : EAD + 1 → EAD dAD → LR
010	dAD (MSB) = 1 : EAD + 1 → EAD dAD → LR
011	EAD − P → EAD dAD (MSB) = 1 : EAD + 1 → EAD dAD → LR
100	EAD − P → EAD
101	EAD − P → EAD dAD (LSB) = 1 : EAD − 1 → EAD dAD → RR
110	dAD (LSB) = 1 : EAD + 1 → EAD dAD → RR
111	EAD + P → EAD dAD (LSB) = 1 : EAD + 1 → EAD dAD → RR

Where P = Pitch, LR = Left Rotate, RR = Right Rotate
EAD = Execute Word Address
dAD = Dot Address stored in the Mask Register

For the various figures, the effect of the initial direction upon the resulting drawing is shown below:



Drawing Parameters

In preparation for graphics figure drawing, the GDC's Drawing Processor needs the figure type, direction and drawing parameters, the starting pixel address, and the pattern from the microprocessor. Once these are in place within the GDC, the Figure Draw command, FIGD, initiates the drawing operation. From that point on, the system microprocessor is not involved in the drawing process. The GDC Drawing Processor coordinates the RMW circuitry and address registers to draw the specified figure pixel by pixel.

The algorithms used by the processor for figure drawing are designed to optimize its drawing speed. To this end, the specific details about the figure to be drawn are reduced by the microprocessor to a form conducive to high-speed address calculations within the GDC. In this way the repetitive, pixel-by-pixel calculations can be done quickly, thereby minimizing the overall figure drawing time. The table below summarizes the parameters.

	DC	D	D2	D1	DM
Initial Value	0	8	8	−1	−1
Line	ΔX	2|ΔY|—|ΔX|	2|ΔY|—2|ΔX|	2|ΔY|	–
Circle	r/√2↑	r-1	2(r-1)	−1	0
Arc	r/√2↑	r-1	2(r-1)	−1	r sinΘ ↓
Rectangle	3	A*	B*	−1	A*
Character	7	–	–	–	–
Area Fill	B**	A**	–	–	–
DMA	L	I	–	–	–
R/W DAT	W	–	–	–	–

Graphics Figure Drawing Parameters

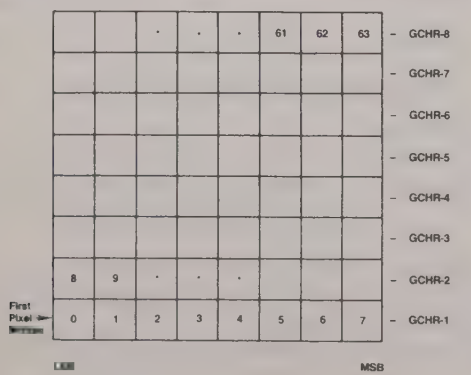
WHERE:

- ΔX = # of pixel positions in the line horizontally.
- ΔY = # of pixel positions in the line vertically.
- r = Radius of the curve, in pixels.
- ↑ = Rounded up to the next higher integer.
- Θ = The angle subtended from the octant axis to the arc.
- A* = The length − 1, in pixels, in the direction initially specified.
- B* = The length − 1, in pixels, in the direction at right angles to the initial direction.
- A** = # of pixels in the initial direction.
- B** = # of pixels in the right angle direction − 1.
- L = # of word address in the perpendicular direction for DMA.
- I = # of DMA transfers in the initially specified direction.
- W = # of word addresses to be written into.
- DC = Drawing Count.
- DM = Dots Masked Count.

Graphics Character Drawing

Graphics characters can be drawn into display memory pixel-by-pixel. The 8-by-8 character is loaded into the GDC's parameter RAM by the system microprocessor. Consequently, there are no limitations on the character set used. By varying the drawing parameters and drawing direction, numerous drawing options are available. In area fill applications, a character can be written into display memory as many times as desired without reloading the parameter RAM.

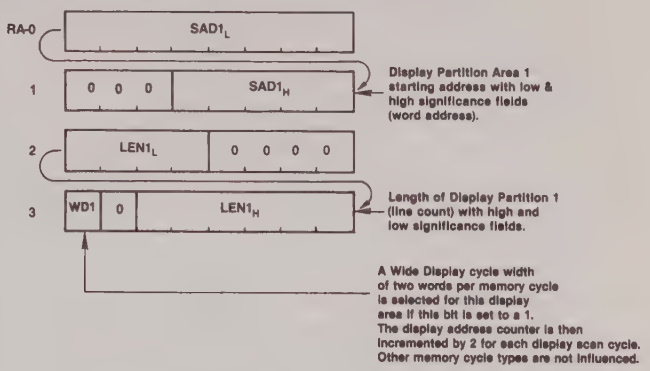
Once the parameter RAM has been loaded with the eight graphics character bytes by the appropriate PRAM command, the GCHRD command can be used to draw the eight bytes into display memory starting at the cursor. The zoom magnification factor for writing, set by the zoom command, controls the size of the character written into the display memory in integer multiples of 1 through 16. The bit values in the PRAM are repeated horizontally and vertically the number of times specified by the zoom factor. As seen in display memory, the writing is started in the lower left corner of the eventual 8-by-8 block and proceeds right to left and bottom to top. The LSBs of the stored character bytes are written first, and parameter RAM location 15 is the first byte to go out.

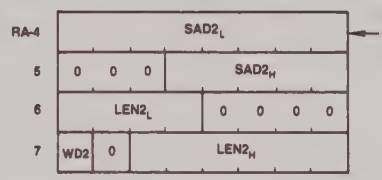


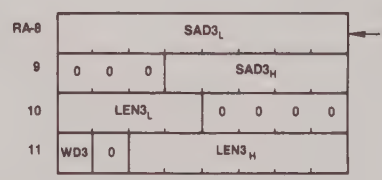
Display Memory

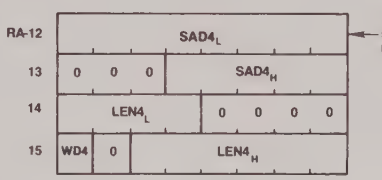
Parameter Ram Contents

Character Mode: RAM Address RA 0 to 16

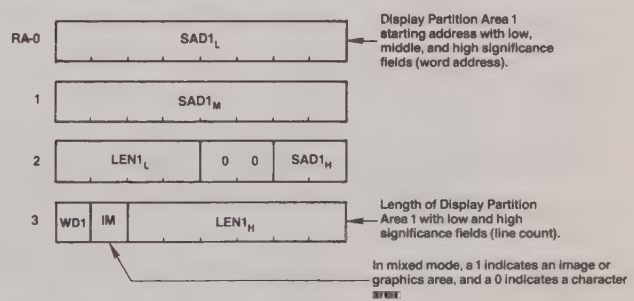

RA-0
SAD1L
1
0 0 0
SAD1H
Display Partition Area 1 starting address with low & high significance fields (word address).
2
LEN1L
0 0 0 0
3
WD1
0
LEN1H
Length of Display Partition 1 (line count) with high and low significance fields.
A Wide Display cycle width of two words per memory cycle is selected for this display area if this bit is set to a 1. The display address counter is then incremented by 2 for each display scan cycle. Other memory cycle types are not influenced.

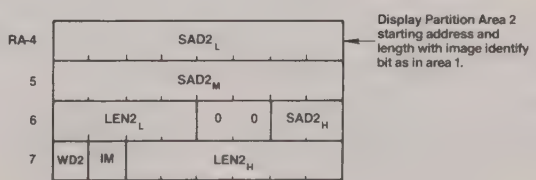


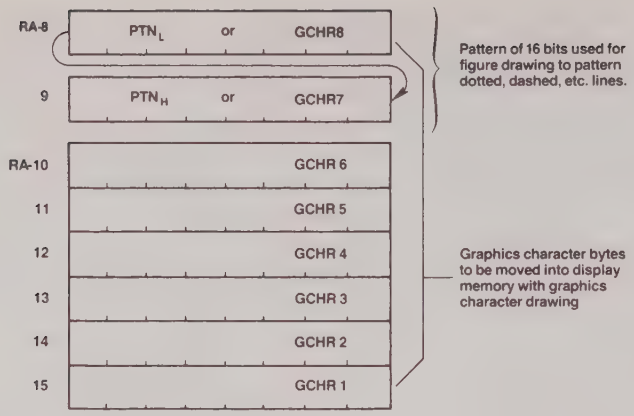




Graphics and Mixed Graphics and Characters Mode







Command Bytes Summary

RESET:	0	0	0	0	0	0	0	0
VSYNC:	0	1	1	0	1	1	1	M
CCHAR:	0	1	0	0	1	0	1	1
START:	0	1	1	0	1	0	1	1
ZOOM:	0	1	0	0	0	1	1	0
CURS:	0	1	0	0	1	0	0	1
PRAM:	0	1	1	1	SA			
PITCH:	0	1	0	0	0	1	1	1
WDAT:	0	0	1	TYPE		0	MOD	
MASK:	0	1	0	0	1	0	1	0
FIGS:	0	1	0	0	1	1	0	0
FIGD:	0	1	1	0	1	1	0	0
GCHRD:	0	1	1	0	1	0	0	0
RDAT:	1	0	1	TYPE		0	0	0
CURD:	1	1	1	0	0	0	0	0
LPRD:	1	1	0	0	0	0	0	0
DMAR:	1	0	1	TYPE		1	0	0
DMAW:	0	0	1	TYPE		1	MOD	

Video Control Commands

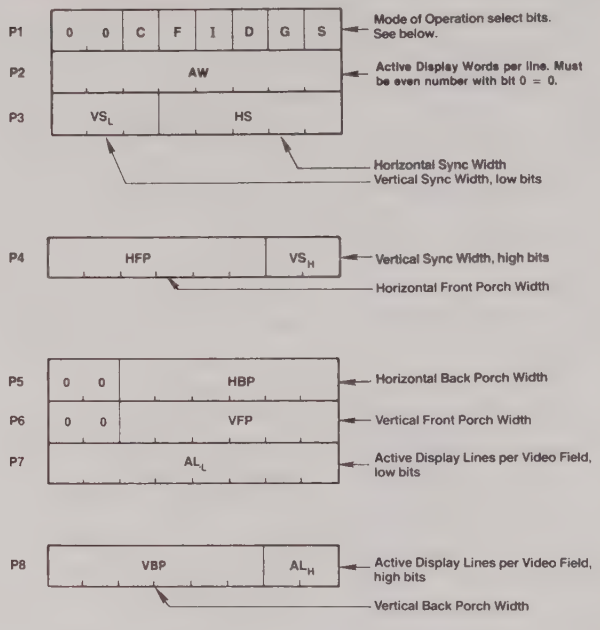
Reset

RESET:	0	0	0	0	0	0	0	0

Blank the display, enter idle mode, and initialize within the GDC:
- FIFO
- Command Processor
- Internal Counters

This command can be executed at any time and does not modify any of the parameters already loaded into the GDC.

If followed by parameter bytes, this command also sets the sync generator parameters as described below.
Idle mode is exited with the START command.


P1 0 0 C F I D G S
Mode of Operation select bits. See below.
P2 AW
Active Display Words per line. Must be even number with bit 0 = 0.
P3 VS$_L$ HS
Horizontal Sync Width
Vertical Sync Width, low bits
P4 HFP VS$_H$
Vertical Sync Width, high bits
Horizontal Front Porch Width
P5 0 0 HBP
Horizontal Back Porch Width
P6 0 0 VFP
Vertical Front Porch Width
P7 AL$_L$
Active Display Lines per Video Field, low bits
P8 VBP AL$_H$
Active Display Lines per Video Field, high bits
Vertical Back Porch Width

In graphics mode, a word is a group of 16 pixels. In character mode, a word is one character code and its attributes, if any.
The number of active words per line must be an even number from 2 to 256.
An all-zero parameter value selects a count equal to 2^n where n=number of bits in the parameter field.
All horizontal widths are counted in display words.
All vertical widths are counted in lines.

Modes of Operation Bits

C	G	Display Mode
0	0	Mixed Graphics & Character
0	1	Graphics Mode
1	0	Character Mode
1	1	Invalid

I	S	Video Framing
0	0	Non-Interlaced
0	1	Invalid
1	0	Interlaced Repeat Field for Character Displays
1	1	Interlaced

Repeat Field Framing: 2 Field Sequence with ½ line offset between otherwise identical fields.

Interlaced Framing: 2 Field Sequence with ½ line offset. Each field displays alternate lines.

Non-interlaced Framing: 1 field brings all of the information to the screen.

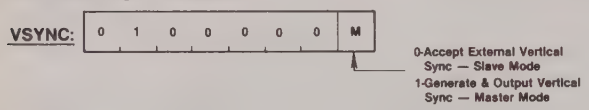
D	Dynamic RAM Refresh Cycles Enable
0	No Refresh — STATIC RAM
1	Refresh — Dynamic RAM

Dynamic RAM refresh is important when high display zoom factors or DMA are used in such a way that not all of the rows in the RAMs are regularly accessed during display raster generation and for otherwise inactive display memory.

F	Drawing Time Window
0	Drawing during active display time and retrace blanking
1	Drawing only during retrace blanking

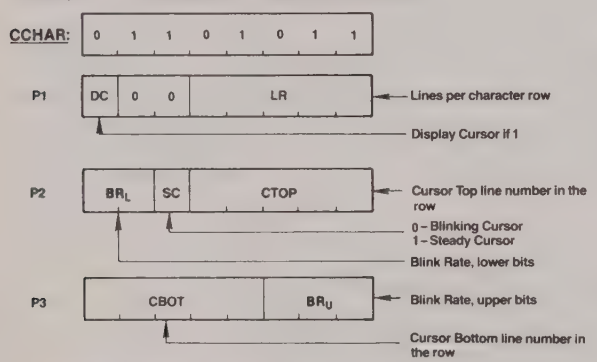
Access to display memory can be limited to retrace blanking intervals only, so that no disruptions of the image are seen on the screen.

Vertical Sync Mode



When using two or more GDCs to contribute to one image, one GDC is defined as the master sync generator, and the others operate as its slaves. The VSYNC pins of all GDCs are connected together.

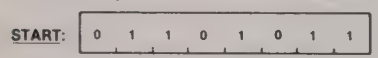
Cursor & Character Characteristics



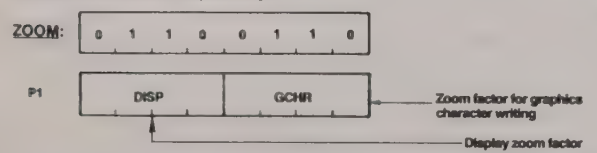
In graphics mode, LR should be set to 1.
The blink rate parameter controls both the cursor and attribute blink rates. The cursor blink-on time = blink-off time = 2 x BR (video frames). The attribute blink rate is always ½ the cursor rate but with a ¾ on-¼ off duty cycle.

Display Control Commands

Start Display & End Idle Mode

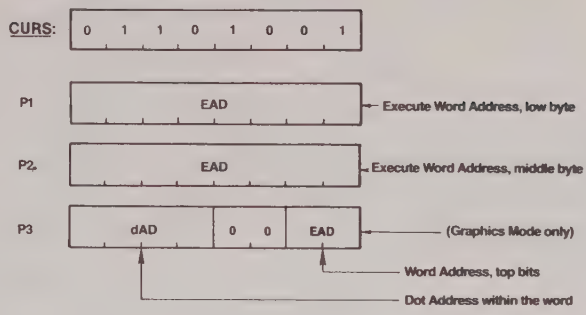


Zoom Factors Specify



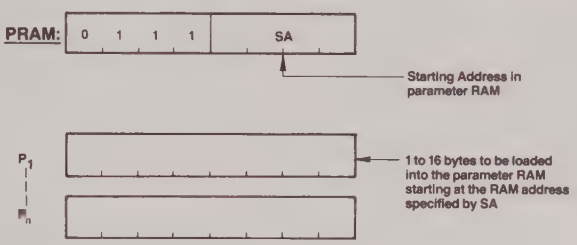
Zoom magnification factors of 1 through 16 are available using codes 0 through 15, respectively.

Cursor Position Specify



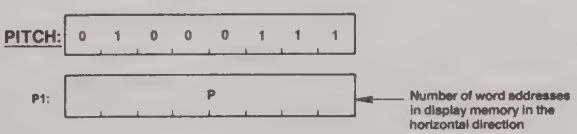
In character mode, the third parameter byte is not needed. The cursor is displayed for the word time in which the display scan address (DAD) equals the cursor address.
In graphics mode, the cursor word address specifies the word containing the starting pixel of the drawing; the dot address value specifies the pixel within that word.

Parameter RAM Load


PRAM:
0 1 1 1 SA
Starting Address in parameter RAM
P1
Pn
1 to 16 bytes to be loaded into the parameter RAM starting at the RAM address specified by SA

From the starting address, SA, any number of bytes may be loaded into the parameter RAM at incrementing addresses, up to location 15. The sequence of parameter bytes is terminated by the next command byte entered into the FIFO. The parameter RAM stores 16 bytes of information in predefined locations which differ for graphics and character modes. See the parameter RAM discussion for bit assignments.

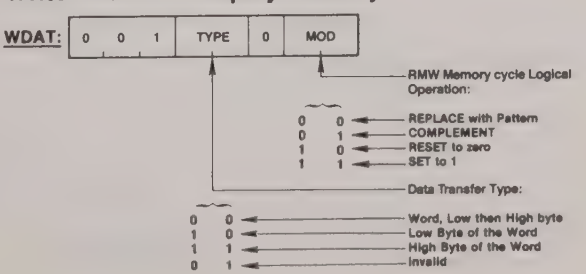
Pitch Specification

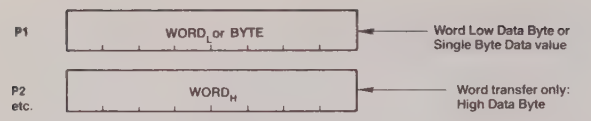


This value is used during drawing by the drawing processor to find the word directly above or below the current word, and during display to find the start of the next line.

Drawing Control Commands

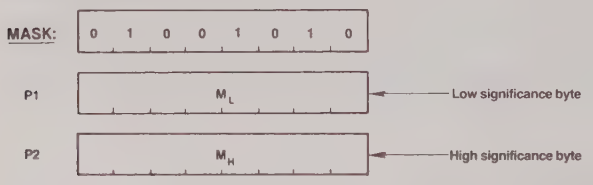
Write Data into Display Memory


WDAT:
0 0 1 TYPE 0 MOD
RMW Memory cycle Logical Operation:
0 0 REPLACE with Pattern
0 1 COMPLEMENT
1 0 RESET to zero
1 1 SET to 1
Data Transfer Type:
0 0 Word, Low then High byte
1 0 Low Byte of the Word
1 1 High Byte of the Word
0 1 Invalid



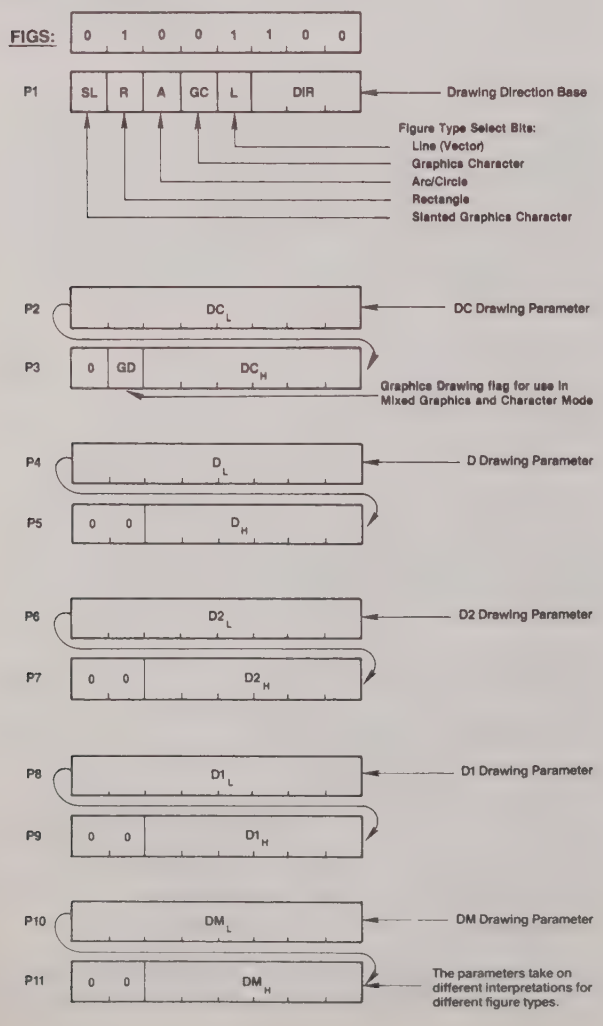
Upon receiving a set of parameters (two bytes for a Word transfer, one for a byte transfer), one RMW cycle into Video Memory is done at the address pointed to by the cursor EAD. The EAD pointer is advanced to the next word, according to the previously specified direction. More parameters can then be accepted.
For byte writes, the unspecified byte is treated as all zeros during the RMW memory cycle.

Mask Register Load



This command sets the value of the 16-bit Mask register of the figure drawing processor. The Mask register controls which bits can be modified in the display memory during a read-modify-write cycle.

Figure Drawing Parameters Specify



Valid Figure Type Select Combinations

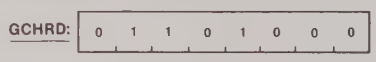
SL	R	A	GC	L	Operation
0	0	0	0	0	Character Display Mode Drawing and Individual Dot Drawing
0	0	0	0	1	Straight Line Drawing
0	0	0	1	0	Graphics Character Drawing and Area filling with graphics character pattern
0	0	1	0	0	Arc and Circle Drawing
0	1	0	0	0	Rectangle Drawing
1	0	0	1	0	Slanted graphics character drawing and slanted area filling

Only these bit combinations assure correct drawing operation.

Figure Draw Start

On execution of this instruction, the GDC loads the parameters from the parameter RAM into the drawing processor and starts the drawing process at the pixel pointed to by the cursor, EAD, and the dot address, dAD.

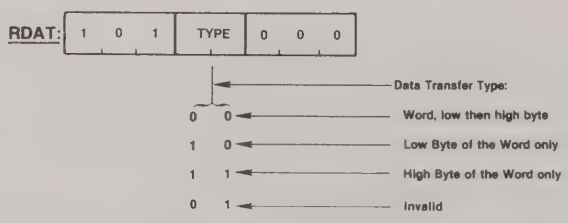
Graphics Character Draw Start



Based on parameters loaded with the FIGS command, this command initiates the drawing of the graphics character or area filling pattern stored in Parameter RAM. Drawing begins at the address in display memory pointed to by the EAD and dAD values.

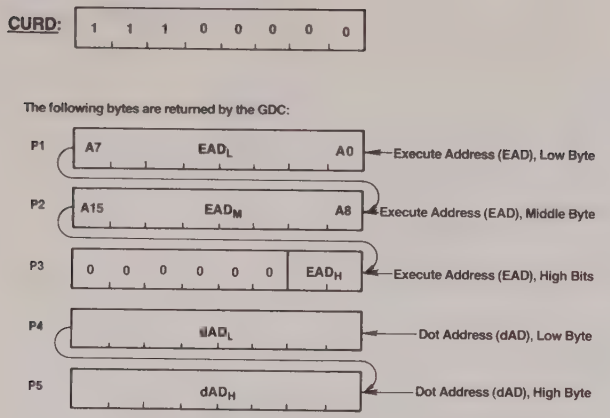
Data Read Commands

Read Data from Display Memory


RDAT: 1 0 1 TYPE 0 0 0
Data Transfer Type:
0 0 Word, low then high byte
1 0 Low Byte of the Word only
1 1 High Byte of the Word only
0 1 Invalid

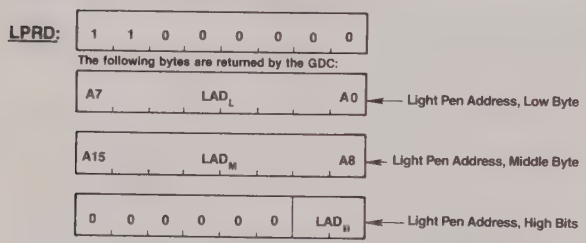
Using the DIR and DC parameters of the FIGS command to establish direction and transfer count, multiple RMW cycles can be executed without specification of the cursor address after the initial load (DC = number of words or bytes + 1).
As this instruction begins to execute, the FIFO buffer direction is reversed so that the data read from display memory can pass to the microprocessor. Any commands or parameters in the FIFO at this time will be lost. A command byte sent to the GDC will immediately reverse the buffer direction back to write mode, and all RDAT information not yet read from the FIFO will be lost.

Cursor Address Read


CURD: 1 1 1 0 0 0 0 0
The following bytes are returned by the GDC:
P1 A7 EAD$_L$ A0 Execute Address (EAD), Low Byte
P2 A15 EAD$_M$ A8 Execute Address (EAD), Middle Byte
P3 0 0 0 0 0 0 EAD$_H$ Execute Address (EAD), High Bits
P4 dAD$_L$ Dot Address (dAD), Low Byte
P5 dAD$_H$ Dot Address (dAD), High Byte

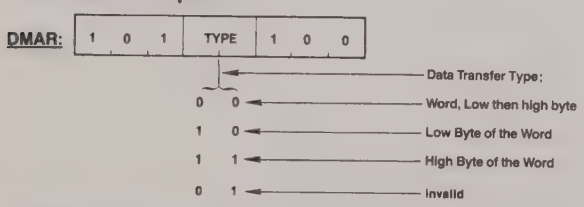
The Execute Address, EAD, points to the display memory word containing the pixel to be addressed.
The Dot Address, dAD, within the word is represented as a 1-of-16 code for graphics drawing operations.

Light Pen Address Read

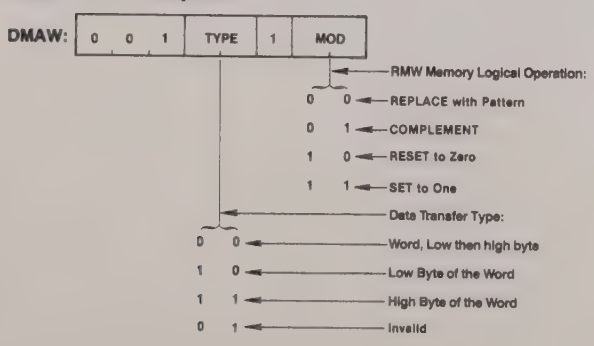

LPRD: 1 1 0 0 0 0 0 0
The following bytes are returned by the GDC:
A7 LAD$_L$ A0 Light Pen Address, Low Byte
A15 LAD$_M$ A8 Light Pen Address, Middle Byte
0 0 0 0 0 0 LAD$_H$ Light Pen Address, High Bits

The light pen address, LAD, corresponds to the display word address, DAD, at which the light pen input signal is detected and deglitched.
The light pen may be used in graphics, character, or mixed modes but only indicates the word address of light pen position.

DMA Read Request



DMA Write Request


DMAW: 0 0 1 TYPE 1 MOD
RMW Memory Logical Operation:
0 0 REPLACE with Pattern
0 1 COMPLEMENT
1 0 RESET to Zero
1 1 SET to One
Data Transfer Type:
0 0 Word, Low then high byte
1 0 Low Byte of the Word
1 1 High Byte of the Word
0 1 Invalid

Absolute Maximum Ratings* (Tentative)

Ambient Temperature under Bias	0°C to 70°C
Storage Temperature	−65°C to 150°C
Voltage on any Pin with respect to Ground	−0.5V to +7V
Power Dissipation	1.5 Watt

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A=0°C to 70°C; Vcc=5V ± 10%

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Input Low Voltage	V_{IL}	−0.5	0.8	V	
Input High Voltage	V_{IH}	2.0	Vcc + 0.5	V	
Output Low Voltage	V_{OL}		0.45	V	I_{OL} = 2.2 mA
Output High Voltage	V_{OH}	2.4		V	I_{OH} = −400 uA
Input Low Leak Current	I_{IL}		−10	uA	V_I = 0V
Input High Leak Current	I_{IH}		+10	uA	V_I = Vcc
Output Low Leak Current	I_{OL}		−10	uA	V_O = 0V
Output High Leak Current	I_{OH}		+10	uA	V_O = Vcc
Clock Input Low Voltage	V_{CL}	−0.5	0.6	V	
Clock Input High Voltage	V_{CH}	3.9	Vcc + 1.0	V	
Vcc Supply Current	I_{CC}		270	mA	

Capacitance

T_A=25°C; Vcc=GND=OV

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Input Capacitance	C_{IN}		10	pF	fc = 1 MHz
I/O Capacitance	$C_{I/O}$		20	pF	V_I (unmeasured) = 0V

AC Characteristics

TA=0°C to 70°C; Vcc=5V ± 10%

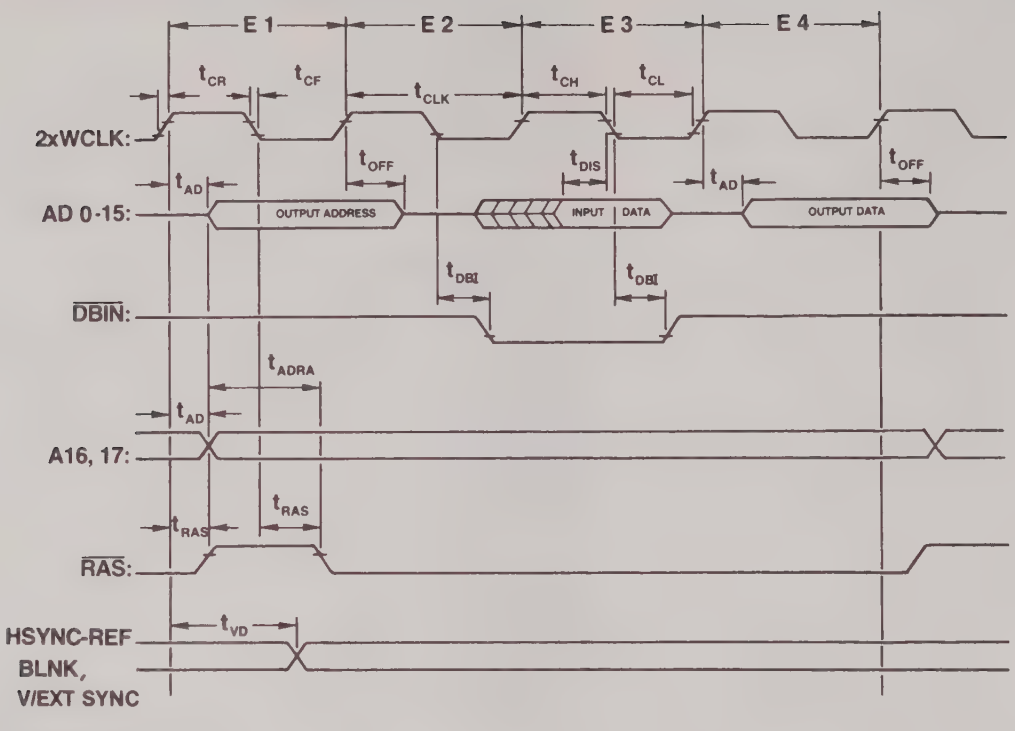
PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Clock Cycle Period	t_{CLK}	167	2000	nS	C_L = 100 pF
Clock High Time	t_{CH}	70		nS	
Clock Low Time	t_{CL}	70		nS	
Clock Rise Time	t_{CR}		10	nS	
Clock Fall Time	t_{CF}		10	nS	
DMA Cycle Time	t_E	4xt_{CLK}		nS	
Data In Set Up Time	t_{DIS}	40		nS	
Data Set Up Time for $\overline{WR}$	t_{DW}	150		nS	
Data Hold Time for $\overline{WR}$	t_{WD}	0		nS	
$\overline{DACK}$ High Level Width	t_{DK}	t_{CLK}		nS	

Timing Requirements

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Address Output Delay	t_{AD}	20	80	nS	C_L = 100 pF
Data Bus In Delay	t_{DBI}		80	nS	
Address Active to $\overline{RAS}$ Low	t_{ADRA}	60		nS	
Video Signal Delay	t_{VD}		120	nS	
$\overline{RD}$ Low to DB Delay	t_{RD}		120	nS	
$\overline{RD}$ High to DB Floating	t_{DF}		120	nS	
$\overline{DACK}$ Low to DRD Delay	t_{DR}		120	nS	
$\overline{RAS}$ Output Delay	t_{RAS}		80	nS	
AD Floating Delay	t_{OFF}		80	nS	

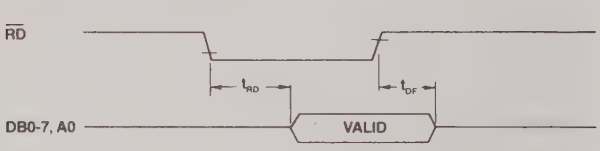
Timing Responses

Display Memory Bus Timing

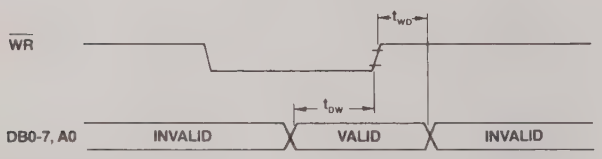


Read-Modify-Write Cycle

Microprocessor Bus Timing

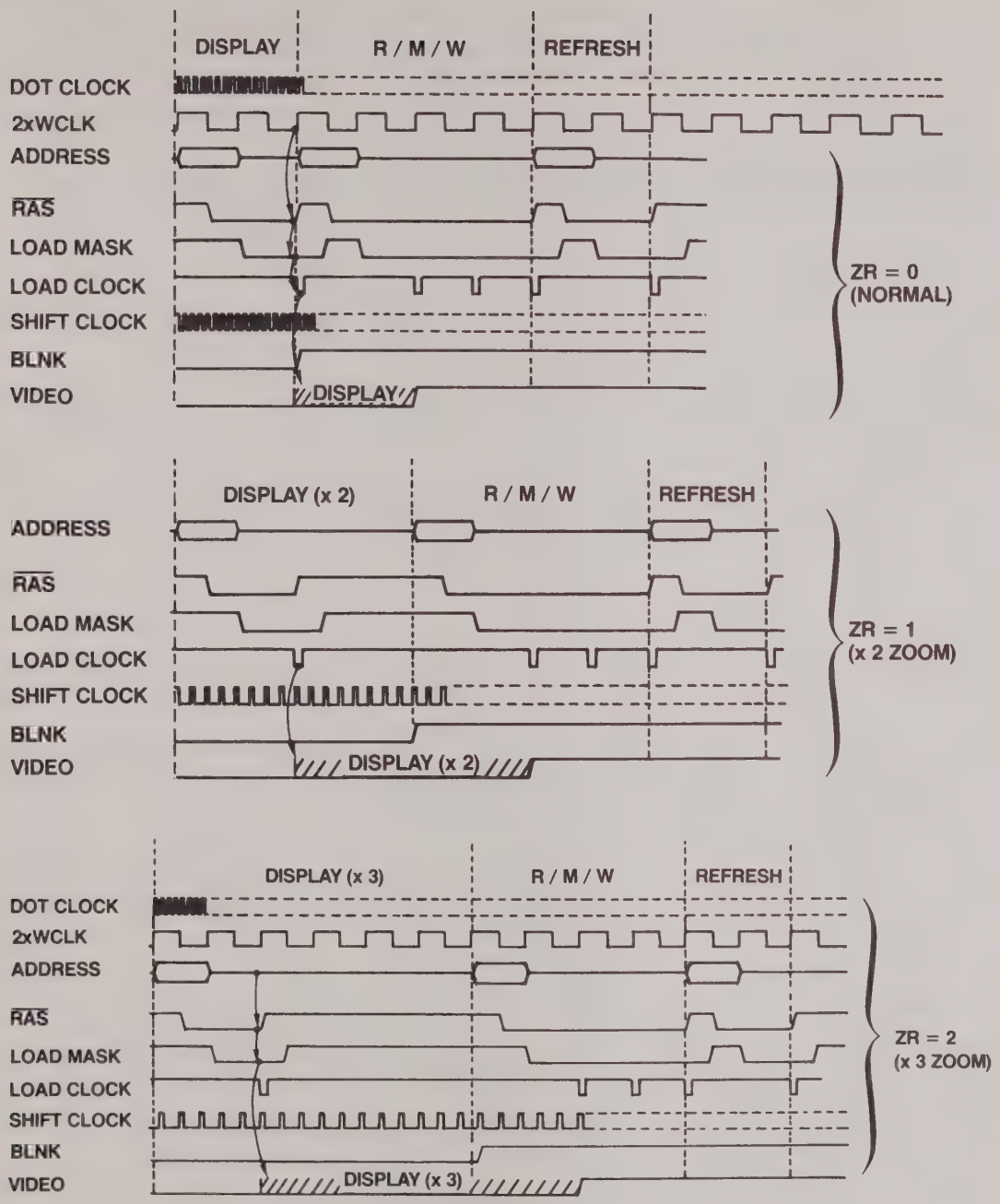


Read Timing

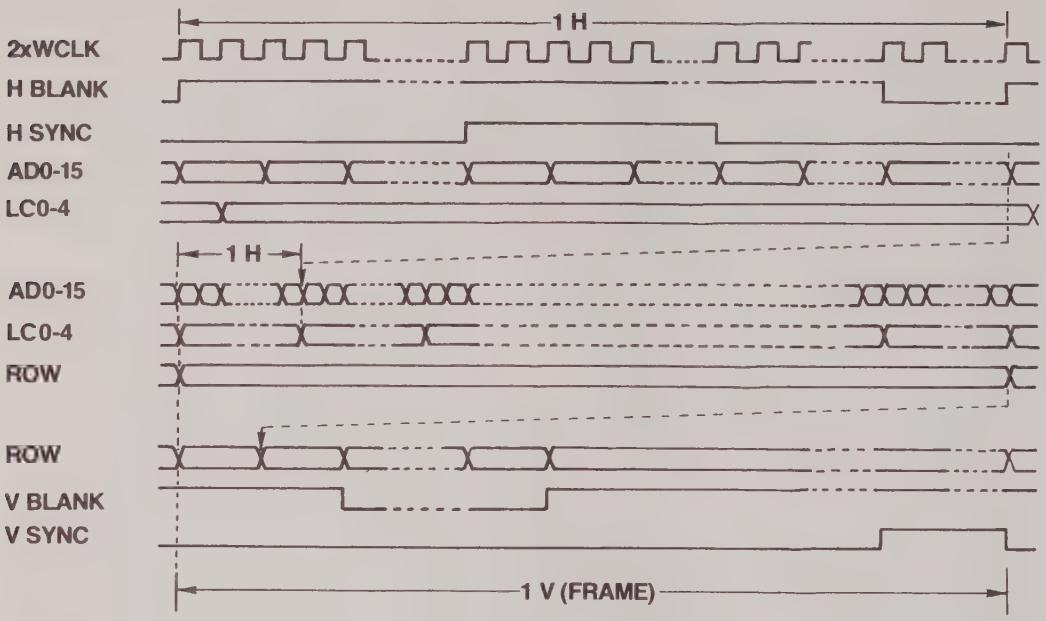


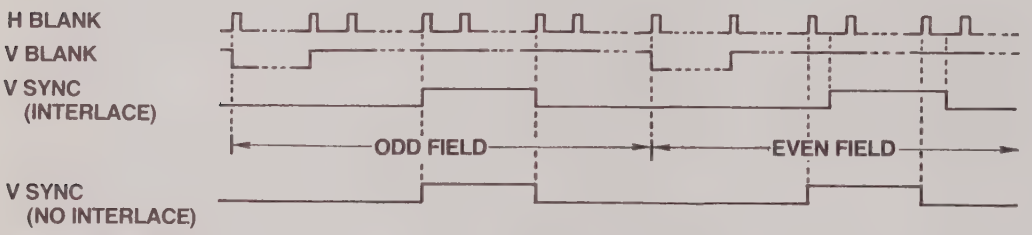
Write Timing

Zoomed Display Timing

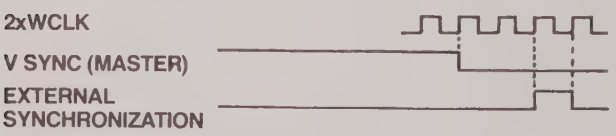


Video Sync Signals Timing



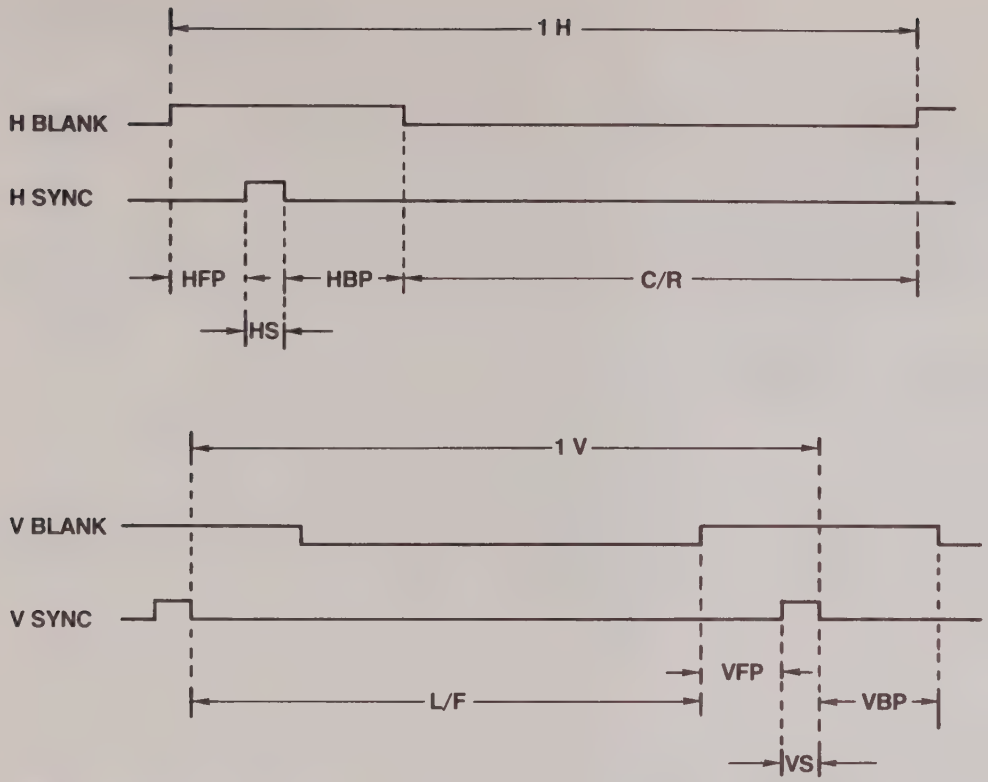


Interlaced Video Timing



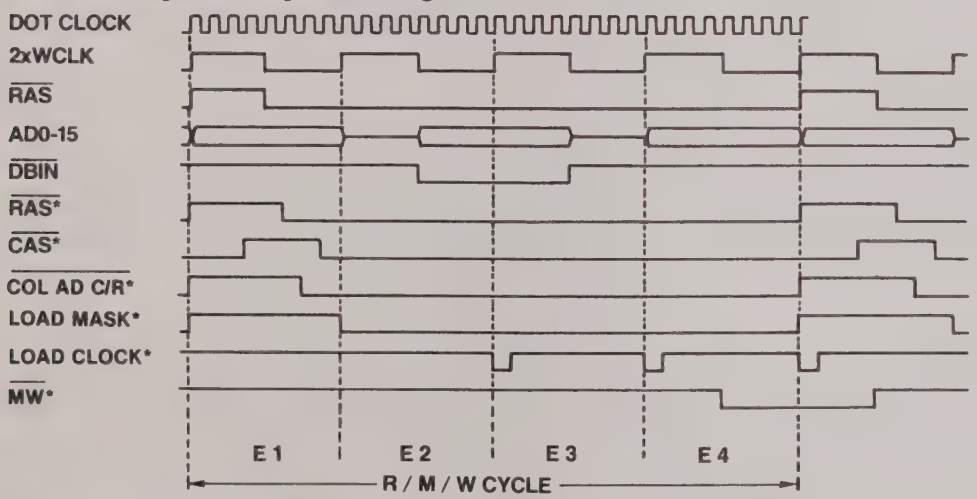
IN SLAVE MODE: HFP ≥ 3

External Synchronization



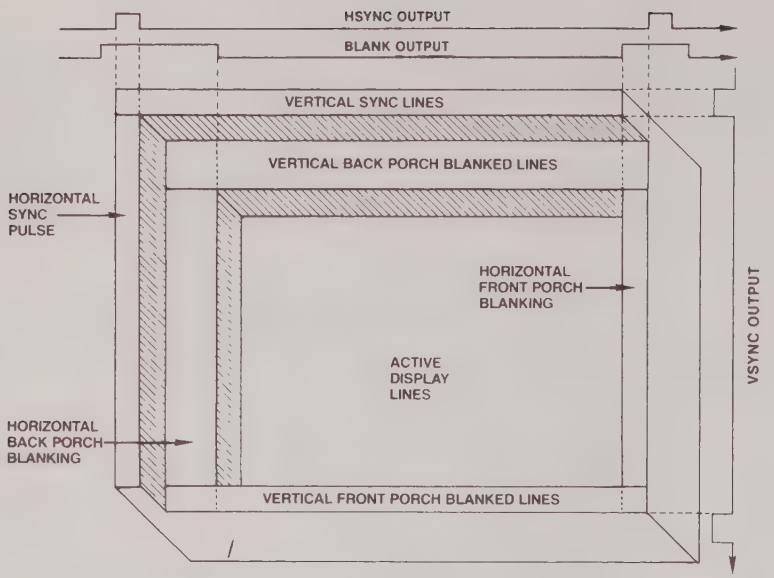
Video Sync Generator Parameters

Read-Modify-Write Cycle Timing

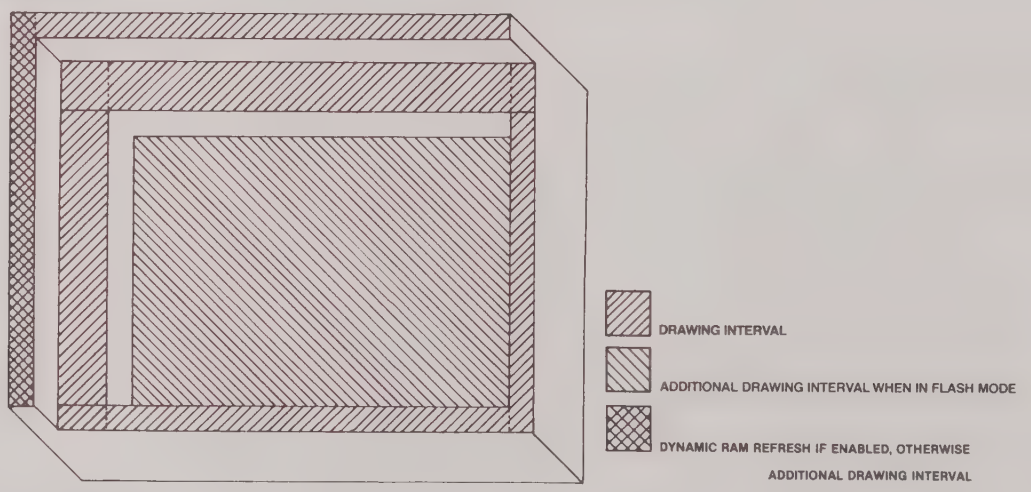


**externally generated signals*

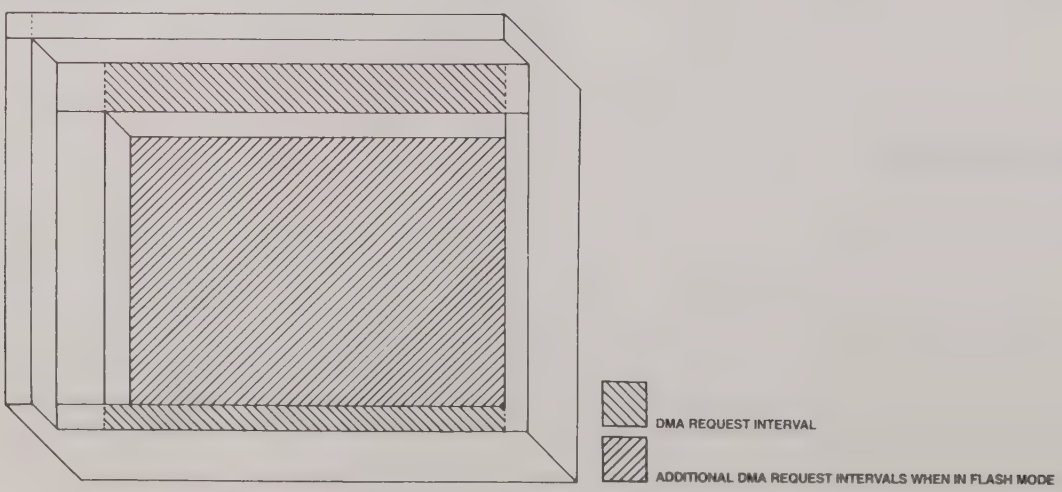
Video Field Timing



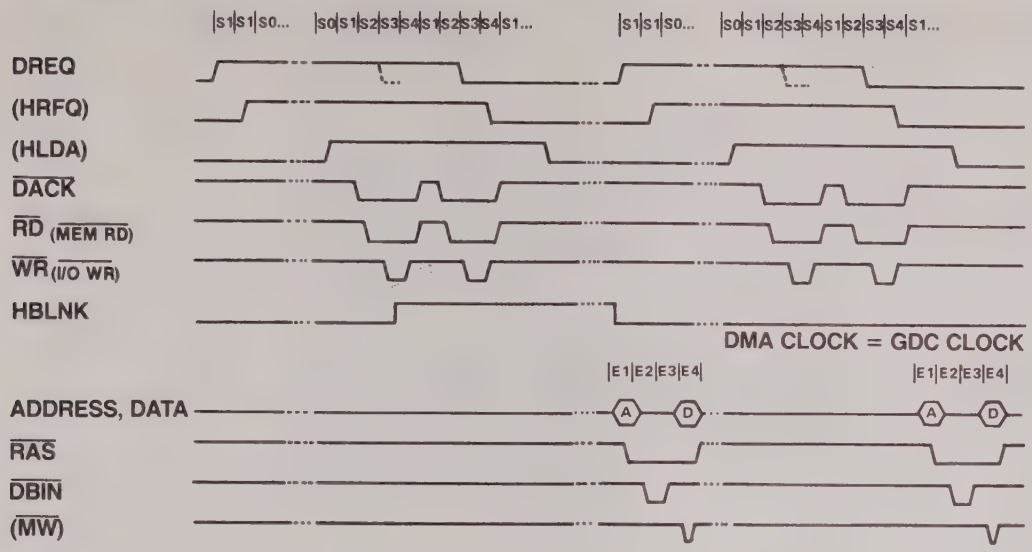
Drawing Intervals


DRAWING INTERVAL
ADDITIONAL DRAWING INTERVAL WHEN IN FLASH MODE
DYNAMIC RAM REFRESH IF ENABLED, OTHERWISE ADDITIONAL DRAWING INTERVAL

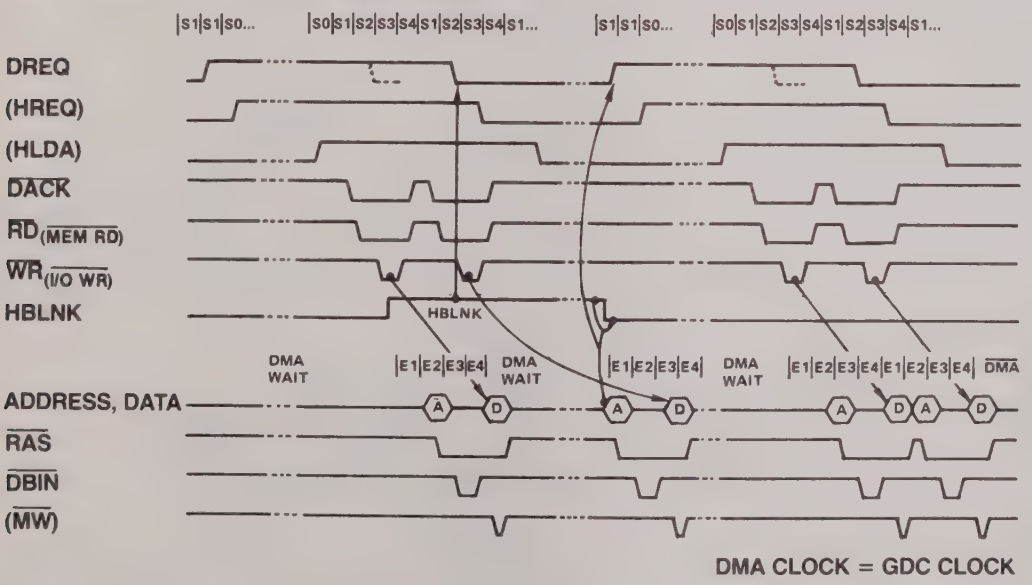
DMA Request Intervals



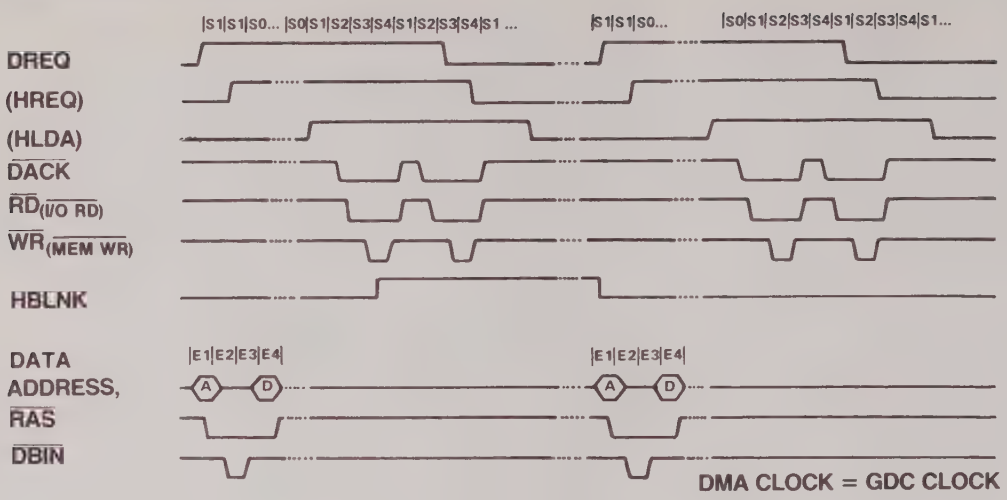
DMA Write (Word) Timing



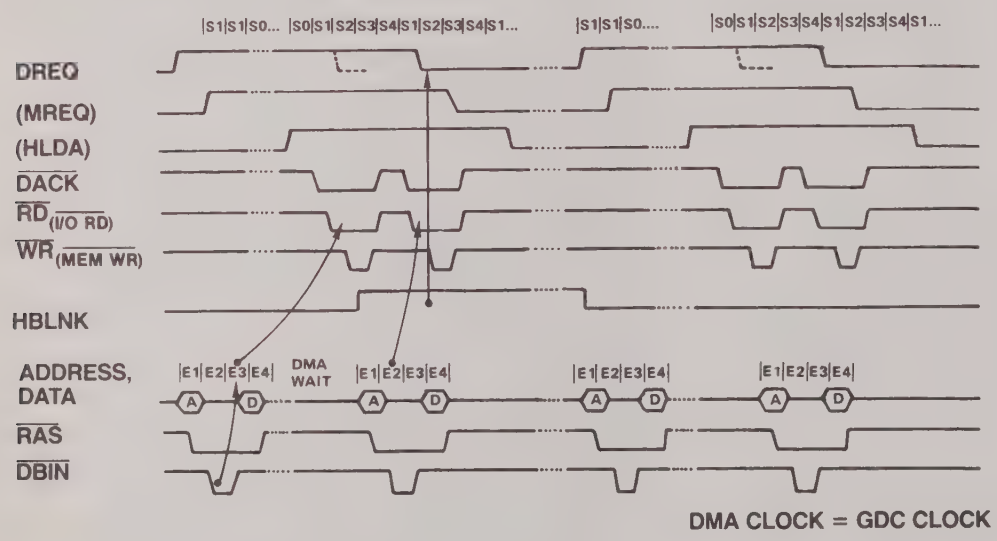
DMA Write (Low Byte, High Byte) Timing



DMA Read (Word) Timing

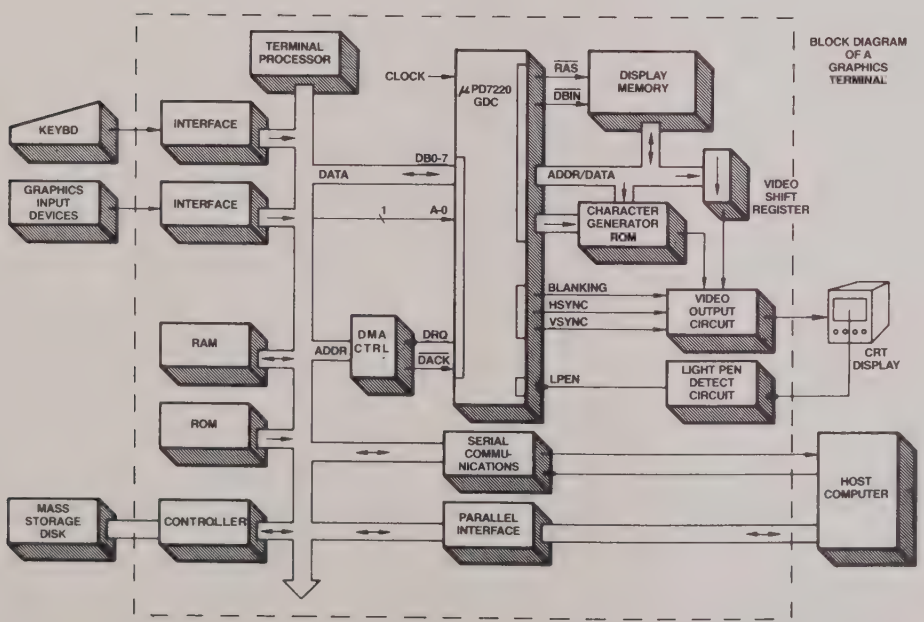


DMA Read (Low Byte, High Byte) Timing

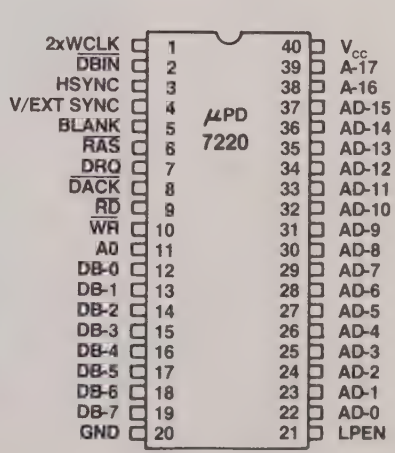


PIN #	PIN NAME	DIRECTION	MODES OF OPERATION		
			GRAPHICS	CHARACTER	MIXED
7	DRQ	OUT	DMA Request Output		
8	$\overline{DACK}$	IN	DMA Acknowledge Input		
12 to 19	DB-0 to 7	IN/OUT	Data Bus to Microprocessor		
11	A0	IN	Address Select Input for Microprocessor Interface		
9	$\overline{RD}$	IN	Read Strobe Input for Microprocessor Interface		
10	$\overline{WR}$	IN	Write Strobe Input for Microprocessor Interface		
3	HSYNC	OUT	Horizontal Video Sync Output		
4	V/EXT SYNC	IN/OUT	Vertical Video Sync Output or External Sync Input		
5	BLANK	OUT	CRT Beam Blanking Output		
1	2xWCLK	IN	Clock Input		
6	$\overline{RAS}$ (ALE)	OUT	Row Address Strobe and Address Latch Enable		
2	$\overline{DBIN}$	OUT	Display Memory Data Bus "Input" Read Cycle Output		
39	A-17	OUT	Address Bit 17 Output	Cursor Output	Cursor & Image Mode Flag
38	A-16	OUT	Address Bit 16 Output	Line Counter Bit 3	Attribute Blink & Clear Line Counter
35 to 37	AD-13 to 15	IN/OUT	Address Bits 13 to 15	Line Counter Bits 0 to 2	Address Bits 13 to 15
22 to 34	AD-0 to 12	IN/OUT	Address and Data Lines to Video Display Memory		
21	LPEN	IN	Light Pen Detect Input		
40	V_{CC}	IN	+5V		
20	GND	IN	Ground		

GDC Pin Names



Block Diagram of a Graphics Terminal



Pin Configuration

NEC
NEC Microcomputers
A Division of NEC Electronics U.S.A. Inc.

173 Worcester Street
Wellesley, Massachusetts 02181
Tel: 617-237-1910 TWX 710-383-1745

The information presented in this document is believed to be accurate and reliable. It is subject to change without notice.

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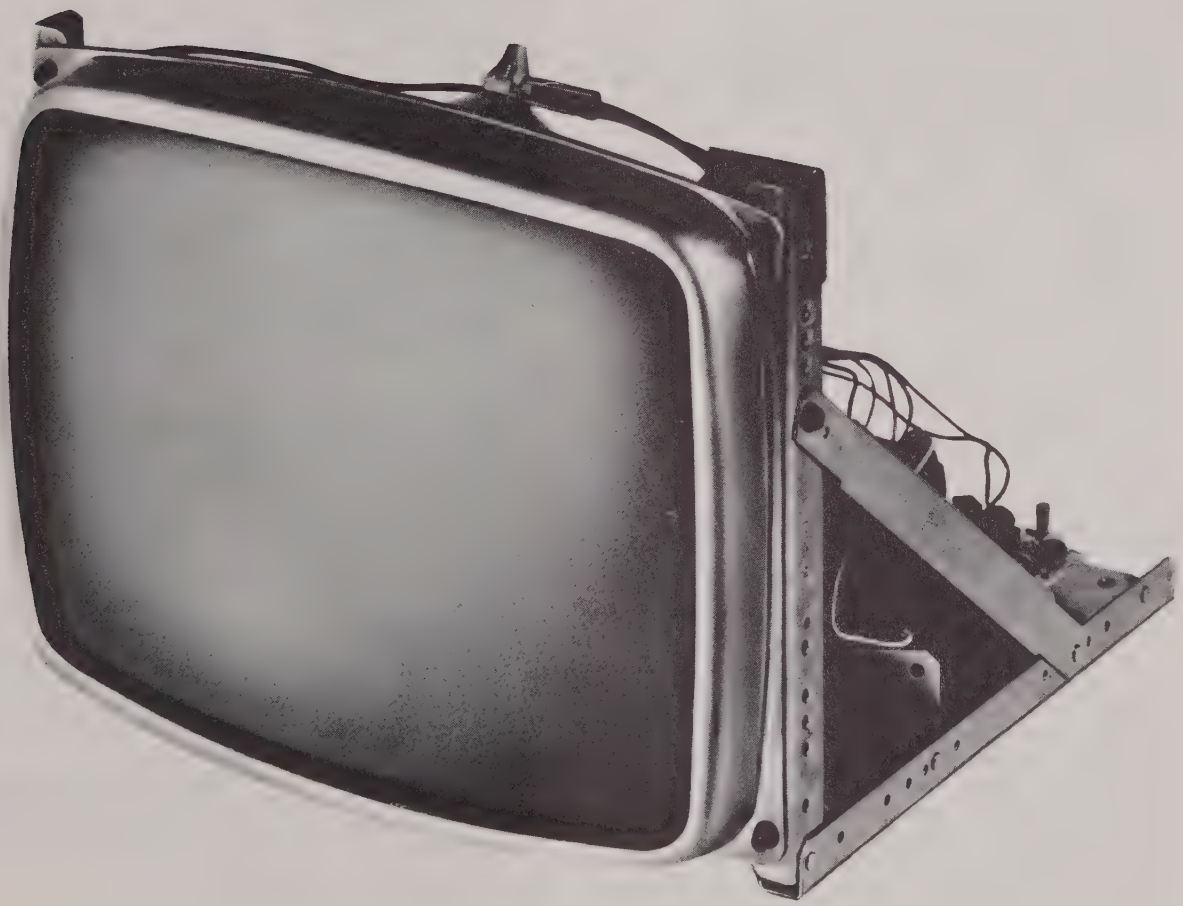
7220DS-6-81-6K

6. TV MONITOR

SERVICE MANUAL



DT2

D12 SERIES DATA DISPLAY TERMINALS

ZENITH RADIO CORPORATION

1000 MILWAUKEE AVENUE, GLENVIEW, ILLINOIS 60025

DT2
2MRR

PRINTED IN U. S. A.
AUG. 1979

$2.00
923-951

PRODUCT SAFETY SERVICING GUIDELINES FOR ZENITH DATA DISPLAY TERMINALS

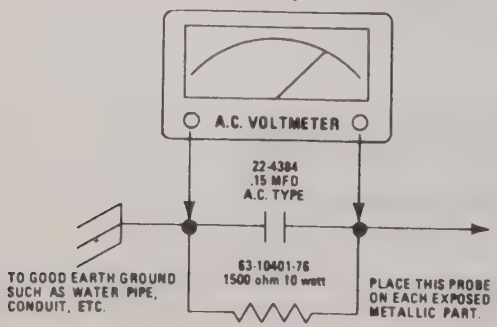
CAUTION: No modification of any circuit should be attempted. Service work should be performed only after you are thoroughly familiar with all of the following safety checks and servicing guidelines. To do otherwise increases the risk of potential hazards and injury to the user.

SAFETY CHECKS

After the original service problem has been corrected, a check should be made of the following:

SUBJECT: FIRE & SHOCK HAZARD

1. Be sure that all components are positioned in such a way to avoid possibility of adjacent component shorts. This is especially important on those chassis which are transported to and from the repair shop.
2. Never release a repair unless all protective devices such as insulators, barriers, covers, shields, strain reliefs, and other hardware have been reinstalled per original design.
3. Soldering must be inspected to uncover possible cold solder joints, frayed leads, damaged insulation, solder splashes or sharp solder points. Be certain to remove all loose foreign material.
4. Check "across-the-line" capacitor (if used) and other components for physical evidence of damage or deterioration and replace if necessary. Follow original layout, lead length and dress.
5. No lead or component should touch a resistor rated at 1 watt or more. Lead tension around protruding metal surfaces must be avoided.
6. **All critical components (shaded on the schematic diagram and parts lists) such as: fuses, flameproof resistors, capacitors, etc., must be replaced with exact Zenith types. Do not use replacement components other than those specified or make unrecommended circuit modifications.**
7. After re-assembly of the terminal always perform an AC leakage test on all exposed metallic parts of the cabinet and screws to be sure the terminal is safe to operate without danger of electrical shock. DO NOT USE A LINE ISOLATION TRANSFORMER DURING THIS TEST. Use an AC voltmeter having 5000 ohms per volt or more sensitivity in the following manner: Connect a 1500 ohm 10 watt resistor (63-10401-76), paralleled by a 0.15 mfd., 150V AC type capacitor (22-4384) between a known good earth ground (water pipe, conduit, etc.) and the exposed metallic parts, one at a time. Measure the AC voltage across the combination 1500 ohm resistor and 0.15 mfd. capacitor. Reverse the AC plug and repeat AC voltage measurements for each exposed metallic part. Voltage measured must not exceed 0.75 volts RMS. This corresponds to 0.5 milliamp AC. Any value exceeding this limit constitutes a potential shock hazard and must be corrected immediately.



SUBJECT: IMPLOSION PROTECTION

1. All Zenith picture tubes are equipped with an integral implosion protection system, but care should be taken to avoid damage during installation. Avoid scratching the tube.
2. Use only Zenith replacement tubes.

SUBJECT: X-RADIATION

1. Be sure procedures and instructions to all service personnel cover the subject of X-radiation. The only potential source of X-rays is the picture tube. However, this tube does not emit X-rays when the HV is at the factory-specified level. It is only when the HV is excessive that X-radiation can be generated. The basic precaution which must be exercised is to keep the HV at the factory-recommended level. Refer to the X-ray Precaution Label which is located inside each terminal for the correct high voltage. The proper value is also given in the schematic diagram. Operation at higher voltages may cause a failure of the picture tube or high voltage supply and, also, under certain circumstances, may produce radiation in excess of desirable levels.
2. Only Zenith-specified CRT anode connectors must be used.
3. It is essential that the serviceman has available at all times an accurate high voltage meter. The calibration of this meter should be checked periodically against a reference standard.
4. When the high voltage circuitry is operating properly there is no possibility of an X-radiation problem. Every time a chassis is serviced, the brightness should be run up and down while monitoring the high voltage with a meter to be certain that the high voltage does not exceed the specified value and that it is regulating correctly. We suggest that you and your service organization review test procedures so that voltage regulation is always checked as a standard servicing procedure, and that the reason for this prudent routine be clearly understood by everyone.
5. When trouble shooting and making test measurements in a terminal with a problem of excessive high voltage, do not operate the chassis longer than is necessary to locate the cause of excessive voltage.

IMPORTANT NOTE: DAG GROUNDING.

Each unit provides for grounding of the main P.C. Board and CRT socket board to the dag of the CRT through the dag grounding spring.

The ground wires are connected to the shell bond or T-band through a terminal lug. Upon installing the Video Display in a terminal, this grounding procedure should be followed to provide adequate high voltage filtering and arc protection. This especially pertains to mounting the video display as a kit version.

CAUTION

NO WORK SHOULD BE ATTEMPTED ON ANY EXPOSED MONITOR CHASSIS BY ANYONE NOT FAMILIAR WITH SERVICING PROCEDURES AND PRECAUTIONS.

GENERAL INFORMATION

This service manual introduces the Zenith D12 series of Video Displays. The series includes three basic forms: the D12-PF which is complete with power supply and frame, the D12-NF without power supply, the D12-NK in kit form which comes without frame or power supply.

The D12 series incorporate precision CRT's which provide uniformity of display and controlled spot size and geometry. The display may be operated from a standard 15 volt D.C. supply (or optional 12 V.D.C.) or from 120 volts A.C.

Input and output connections for the displays are made through a 10 pin edge connector on the main circuit board. Provision has been made for an optional remote brightness control. Schematic reference numbers are printed on the circuit board to aid in the location and identification of components for servicing.

Vertical and horizontal linearity is maintained within specifications without the use of linearity controls or adjustable devices. Excellent vertical linearity is assured by the extensive use of current feedback and horizontal linearity is achieved with a fixed saturable reactor.

Vertical and horizontal deflection systems sustain scan even in the absence or interruption of synchronizing signals. Vertical and horizontal synchronization is automatic and stable throughout the entire specified operating frequency range.

SPECIFICATIONS

CATHODE RAY TUBE

12″ diagonal measure, 90° deflection, I2.5KV nominal high voltage at 50μ A. beam current. Available with bonded anti-reflective face plate option. P4 phosphor is standard and other EIA phosphors are available.

NOMINAL DISPLAY AREA

5I sq. in. defined by a rectangle 8 1/2″ × 6″ centered on the CRT. (Other display dimensions optional.)

INPUT SIGNALS (TTL LEVEL)

HORIZONTAL

4 to 40μ sec. duration (positive going standard).

VERTICAL

50 to 2500μ sec. duration (negative going standard).

VIDEO

1.0V to 2.5V P-P (internal or customer supplied 500Ω contast control for higher input levels).
Positive polarity for white characters. (Other polarities are available for horizontal and vertical sync.)

POWER SUPPLY

120V ± 10% or 240V ± 10%
(customer strappable) 47 to 63 Hz., or
15V DC at 800 ma. max., or
12V DC at 1100 ma. max.

BRIGHTNESS CONTROL

Internal or Customer supplied 100 KΩ potentiometer (accessible at pins 2, 3 and 4 of edge connector).

INTERCONNECT TO CUSTOMER SYSTEM

Via standard 10-pin edge connector.
VIKING #25V10S/1-2
AMP #225-21031-101
CINCH #250-10-30-170

RESOLUTION

900 vertical lines minimum at center of display and 700 vertical lines at the corners. Pulse rise time less than 20 nanoseconds, for 30V rise at CRT. Bandwidth is within 3db from 10 Hz. to 18 MHz.

GEOMETRY

NOTE: Measurements made with an input of 1.0-2.5V P-P and with the display adjusted to 6″ highx8½″ wide.

VERTICAL

a. Height of display at left side shall be within ± 2.0 percent of height at right side.
b. Top and bottom pincushion or barrel shall be within ±1.25% of the average height.

HORIZONTAL

a. Width of display at top shall be within ±2.5% of the width at bottom.
b. Side pincushion or barrel shall be within ± 1.0% of the average width.

LINEARITY

No character shall vary in width or height by more than ±10% of the average width or height of all the characters in a row or column respectively.No specific character shall vary in width or height more than ±10% of an adjacent character.

SYNCHRONIZATION

HORIZONTAL

15.75 ± 0.5KHz.
18.60 ± 0.5KHz. (Optional)

Horizontal Blanking

9.0μ sec. min.

Horizontal Phasing Control

11.0 μ sec. nominal range

VERTICAL

47 to 63 Hz.

VERTICAL RETRACE TIME

850μsec. max.

STORAGE

55° C. max. with bonded anti-reflective faceplate.
65° C. max. for plain faced CRT's.

ENVIRONMENT

Operating temperature

55° max. (free air temperature of display electronics).

Altitude

40,000 ft. + storage & shipment.
10,000 ft. max. operating.

WEIGHT

11.5 lbs. max. without optional power supply.
13.5 lbs. max. with optional power supply.
9.0 lbs. max. without frame.

THEORY OF OPERATION

POWER SUPPLY

Power Transformer TX201 is designed for use with 120V or 240V A.C. source. The secondary provides power to bridge rectifier (CR501, CR502, CR503 and CR504). The positive output of the bridge rectifier (junction of CR503 and CR504), forms the raw B+ supply (~ 20VDC).

Voltage regulation is accomplished in the negative leg of the power supply through a feedback network consisting of transistors QX501 and QX502 and their associated circuitry. The emitter voltage of QX501 is maintained by diodes CR505, CR506 and CR507. The base voltage is provided by potentiometer RX506.

If B+ increases, diodes CR505, CR506 and CR507 will draw more current to maintain the emitter voltage of QX501. Additionally, the voltage developed across RX506 will increase, resulting in a higher positive voltage at the base of QX501 which will result in less conduction. This reduces the base current of QX502 since QX501 provides the emitter/base current path for QX502. When QX502 conducts less, the voltage drop across Q502 is increased thus lowering B+.

If B+ decreases, diodes CR505, CR506 and CR507 will reduce conduction to maintain the emitter voltage of QX501. Additionally, the base voltage provided by RX506 will decrease. Less voltage on the base of QX501 will cause it to increase conduction, resulting in a greater emitter/base current flow in QX502. With this condition the voltage drop for Q502 is less and B+ is increased.

HORIZONTAL

The low-level horizontal section, which consists of transistors Q101 and Q102 (and associated circuitry), functions as a variable time delay monostable multivibrator. The input trigger for this circuit is provided by the horizontal drive pulse. The pulse is injected into the base or emitter (for either positive or negative pulse respectively) of Q101 through injection network C101, C111, R101, R110 and CR101. By varying the recovery time of the multivibrator, potentiometer R104 adjusts video information position (with respect to raster scan). Output of the monostable multivibrator, derived at the collector of Q102, is injected through a coupling network consisting of C110 and CR103. The resulting "Lock" signal is rereceived by one side of a precision astable multivibrator at the emitter of Q103. The astable multivibrator circuit is completed through Q104 and associated circuitry. This circuit will act as a free running oscillator until the "Lock" signal is received from the previous stage. Once locked, an output pulse is formed at the emitter of Q104 which is then D.C. coupled to the base of the horizontal driver transistor, Q105.

Remainder of the horizontal circuit is straightforward. Features to be noted are: Width and Linearity Coils LX102 and LX101 in series with the yoke (TX202). Linearity is fixed and an adjustable coil is provided for width. The linearity coil has a magnetically biased core which makes the inductance of the coil dependent upon its current. Pincushion and geometric corrections are made at the factory by the addition of rubber magnets around the plastic ring of the yoke. D.C. operation of 12 volts is accomplished by the (optional) addition of a boost circuit at the horizontal sweep transformer.

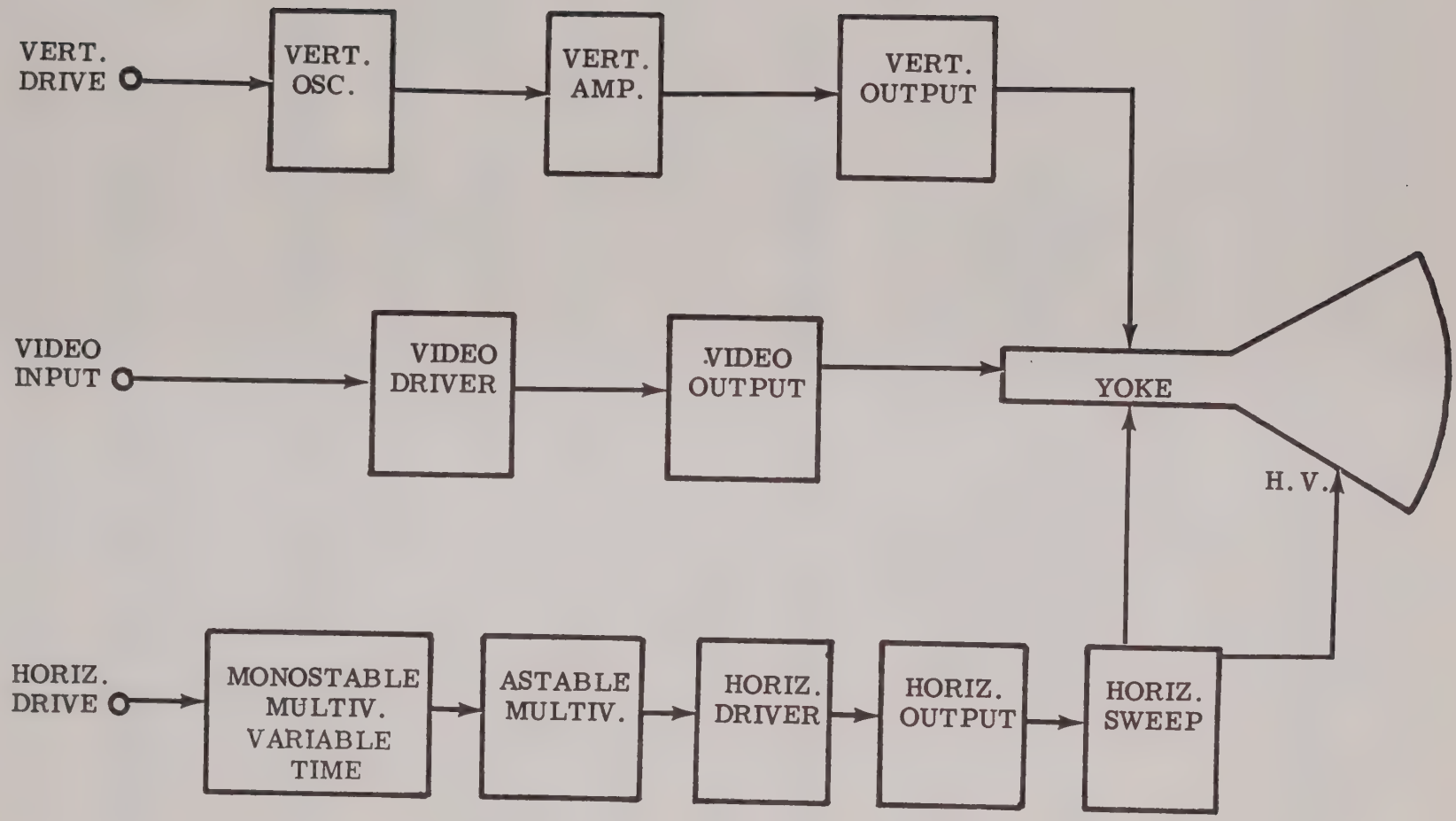
VERTICAL

The vertical circuit includes an oscillator consisting of transistors Q301 and Q302 and associated circuitry. Amplification is provided by transistors Q303 and Q304 with the emitter of Q304 feeding the base of the vertical driver Q305. The vertical output transistors, Q306 and Q307 are wired in the standard push-pull configuration. Transistor Q308 doubles B+ during retrace, maintaining less than 800 μ sec. of retrace time.

VIDEO

The video amplifier circuit consists of transistors Q401 and Q402 and associated circuitry. The circuit comprises a cascode amplifier which is triggered by a positive pulse at pin 8 of the edge connector. Upon receiving the input pulse, conduction is initiated and the collector voltage of Q402 is lowered. Amplification of low frequency voltage gain is fixed by the ratio of R407 and R408. Gain is maintained to 18 MHz by the bandwidth enhancing components R406, C403, and L401. Resistors R402 and R403 provide bias for the amplifier.

The collector output of Q401 is D.C. coupled to the cathode of the C.R.T. through resistor R201. Raster cut-off is adjusted with the brightness control R114 which is connected to G1 of the C.R.T.

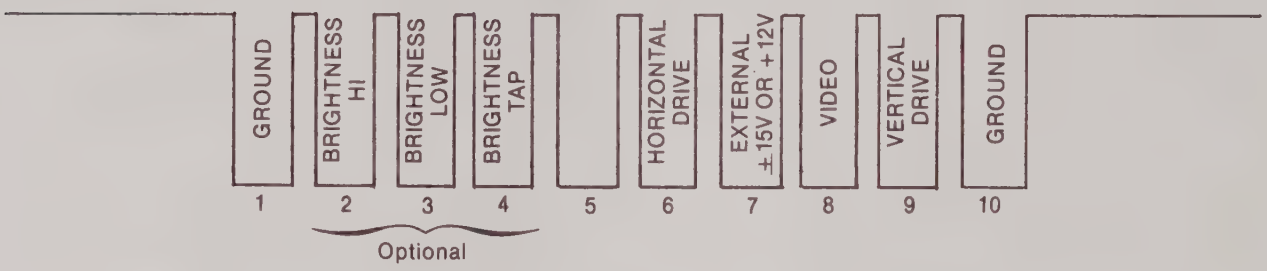

VERT.
DRIVE
VERT.
OSC.
VERT.
AMP.
VERT.
OUTPUT
VIDEO
INPUT
VIDEO
DRIVER
VIDEO
OUTPUT
YOKE
H.V.
HORIZ.
DRIVE
MONOSTABLE
MULTIV.
VARIABLE
TIME
ASTABLE
MULTIV.
HORIZ.
DRIVER
HORIZ.
OUTPUT
HORIZ.
SWEEP

ADJUSTMENT PROCEDURES FOR D12 VIDEO DISPLAY

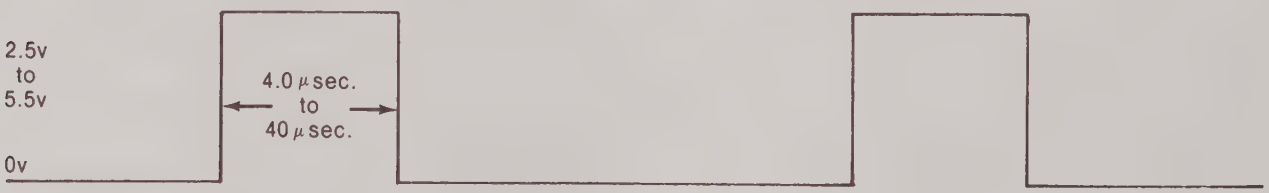
1. External power is applied to the monitor through an AC line cord or a 4 pin molex connector. The unit is wired for 120 VAC 50/60 Hz operation. (240 VAC 50/60 Hz optional)

2. INPUT SIGNALS: Input signals are connected to the display board through a 10 pin edge connector.

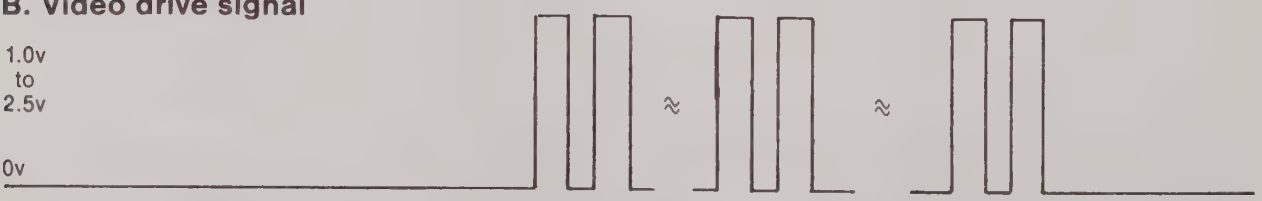
Component Side of Display Board



A. Horizontal drive signal — 15750Hz ± 500Hz, 18,600Hz ± 500Hz

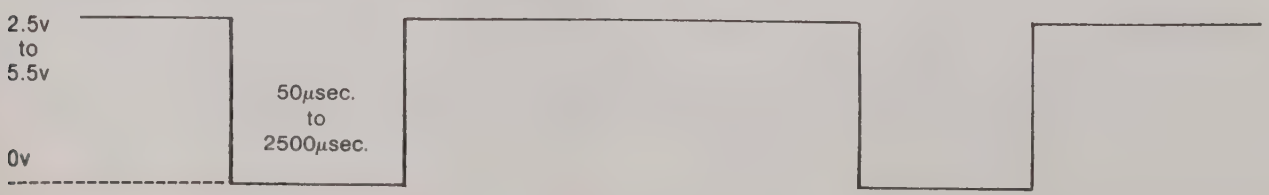


B. Video drive signal

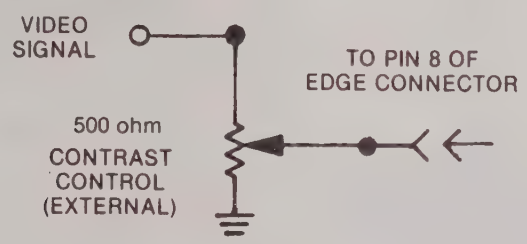


At a horizontal frequency of 15.7KHZ the video drive signal should start 11 microseconds ±5μ sec. after the leading edge of horizontal sync, and 900 microseconds or greater after the leading edge of vertical sync.

C. Vertical drive signal – 47Hz to 63Hz



Should the video drive level exceed the 2.5 volts specified, an external contrast control must be provided. The video drive signal is connected to the top end of the 500Ω pot, the bottom end is grounded and the wiper arm connects to the video input of the edge connector as shown.



3. Once power is applied to the display and the input signals connected, adjust the brightness control until the edges of the raster are visible.

4. Depending on the requirements for height and width of the video presentation, the vertical size control and width coil should be adjusted accordingly.

5. The power supply board also has a control to adjust the regulated B+ of the monitor to +15V. Check for proper adjustment.

6. Adjust the phase control to center the video information within the raster. (The contrast control may have to be adjusted to obtain a display of the video information.)

7. Adjust brightness control for visual cutoff of the raster.

8. Adjust external contrast control for desired luminance.

9. Adjust focus control for best possible overall focus.

IMPORTANT NOTE: DAG GROUNDING.

Each unit provides for grounding of the main P.C. Board and CRT socket board to the dag of the CRT through the dag grounding spring.

The ground wires are connected to the shell bond or T-band through a terminal lug. Upon installing the Video Display in a terminal, this grounding procedure should be followed to provide adequate high voltage filtering and arc protection. This especially pertains to mounting the video display as a kit version.

VIDEO BOARD & CRT SOCKET

L102 HORIZ. WIDTH
YOKE
YEL
L101 H. LIN.
C116
C110
C114
C115
CR103
CR105
CR108
CRT
BK
R104 VIDEO-HORIZ. PHASE
R105
R107
R108
R109
R111
R112
R113
R114
R115
R116
R117
R122
R123
R124
R125
R126
R127
C101
C102
C103
C104
C105
C106
C107
C108
C109
C111
C112
C113
C117
C118
C120
C121
Q101
Q102
Q103
Q104
Q105
Q106
CR101
CR102
T101
L401
C401
R401
R402
R403
R404
R405
R407
R408
R410
R411
R413
R415
R416
R417
R418
C402
C403
C404
Q401
Q402
CR104
CR107
CR401
R409
R412
R419
R421
BRITE
FOCUS
CRT Y
CRT Y-O
CRT BL
CRT Y-G
BR CRT
C311
R323
R324
C312
CR304
Q306
VERT. YOKE
C313
R312
VERT SIZE R309
R313
C307
R316
R314
Q304
R315
C306
C309
R321
Q307
R322
C308
CR305
Q305
R318
R310
R308
C314
R325
W-R
Q301
R319
R301
Q303
C305
R311
Q308
R307
R320
R304
R306
C304
C303
R305
R303
C302
C301
R302
Q302
GND. P.S.
BK
C310
B+ P.S.
B+
R202
CRT
BR
10

LEGEND

ITEM NO.	PART NO.	DESCRIPTION	
C101	22-7614-08A	330 PFD. CAPACITOR ±20% DISC.	50V
C102	22-7619-39A	180 PFD CAPACITOR ±5% DISC. NPO	50V
C103	22-7619-39A	180 PFD. CAPACITOR ±5% DISC. NPO	50V
C104	22-7622-28A	56 PFD CAPACITOR ±10% DISC NPO	50V
C105	22-7619-39A	180 PFD CAPACITOR ±5% DISC NPO	50V
C106	22-7619-39A	180 PFD CAPACITOR ±5% DISC NPO	50V
C107	22-7619-39A	180 PFD CAPACITOR ±5% DISC NPO	50V
C108	22-7619-39A	180 PFD CAPACITOR ±5% DISC NPO	50V
C109	22-7152-03	4.7 MFD CAPACITOR ELEC. +100%-10%	25V
C110	22-7613-04A	220 PFD CAPACITOR ±10% DISC	50V
C111	22-7622-28A	56 PFD CAPACITOR ±10% DISC	50V
C112	22-7614-24A	.01 MFD CAPACITOR ±20% DISC	50V
C113	22-7440	.0047 MFD CAPACITOR ±10% DISC	500V
CX114	22-7530-07	.015 MFD CAPACITOR SPECIAL..	
C115	22-7656-13A	22 PFD CAPACITOR ±10% DISC	50V
C116	22-7313	10 MFD CAPACITOF SPECIAL	
C117	22-7719-09	100 MFD CAPACITOR ±20% ELEC.	35V
C118	22-3748	.001 MFD CAPACITOR ±10% DISC	1KV
C120	22-7722-02	2.2 MFD CAPACITOR, ±20% ELEC.	100V
C121	22-7722-01	1 MFD CAPACITOR, ±20% ELEC.	100V
C122	22-7613-09	560 PFD CAPACITOR ±10% DISC.	50V
C123	22-7613-09	560 PFD CAPACITOR ±10% DISC.	50V
C301	22-7613-24A	.01 MFD CAPACITOR ±10% DISC	50V
C302	22-7548	.15 MFD CAPACITOR ±10% POLYESTER	50V
C303	22-7152-05	22 MFD CAPACITOR +100-10% ELEC.	25V
C304	22-7720-09	100 MFD CAPACITOR ±20% ELEC. 105°C	50V
C305	22-7579-03	4.7 MFD CAPACITOR ELEC. ±10%	16V
C306	22-7613-02A	150 PFD CAPACITOR ±10% DISC	50V
C307	22-7389-02	1MFD CAPACITOR ±20% ELEC.	25V
C308	22-7718-08	47 MFD CAPACITOR ±20% ELEC.	25V
C309	22-7152-04	10 MFD CAPACITOR ±100-10% ELEC 105°C	25V
C310	22-7614-18A	.0033 MFD CAPACITOR ±20% DISC	50V
C311	22-7613-25A	.012 MFD CAPACITOR ±10% DISC	50V
C312	22-7579-04	1000 MFD CAPACITOR ±10% ELEC.	16V
C313	22-7389-02	1 MFD CAPACITOR ±20% ELEC	25V
C314	22-7614-20A	.0047 MFD CAPACITOR ±20% DISC	50V
C401	22-7722-08	47 MFD CAPACITOR ±20% ELEC. 105°C	100V
C402	22-7721-04	4.7 MFD CAPACITOR ±20% ELEC. 105°C	63V
C403	22-7613A	100 PFD CAPACITOR ±10% DISC	50V
C404	22-7724	.02 MFD. CAPACITOR +80-20% DISC.	500V
C405	22-3512	.01 MFD CAPACITOR +40-10% DISC	1KV
R101	63-9822	15K OHM RESISTOR ±5% FILM	1/4W
R102	63-9819-94	8.2K OHM RESISTOR ±2% FILM	1/4W
R103	63-9919-94	8.2K OHM RESISTOR ±2% FILM	1/4W
R104	63-10651-11	CONTROL 25K OHM (HORIZ. PHASE)	
R105	63-10533-05	357K OHM RESISTOR ±1% METAL FILM	1/4W
R106	63-9922-14	56K OHM RESISTOR ±5% FILM	1/4W
R107	63-10533-04	267K OHM RESISTOR ±1% METAL FILM	1/4W
R108	63-9921-94	8.2K OHM RESISTOR ±5% FILM	1/4W
R109	63-9921-94	8.2K OHM RESISTOR ± 5% FILM	1/4W
R110	63-9921-66	560 OHM RESISTOR ±5% FILM	1/4W
R111	63+0351-89	5.1KOHM RESISTOR ±2% FILM	1/4W
R112	63-9919-84	3.3KOHM RESISTOR ± 2%FILM	1/4W
R113	63-10533-04	267K OHM RESISTOR ± 1% METAL FILM	1/4W
R114	63-10533-04	267K OHM RESISTOR ± 1% METAL FILM	1/4W
R115	63-9919-84	3.3K OHM RESISTOR ±2% FILM	1/4W
R116	63-9921-79	2K OHM RESISTOR ±5% FILM	1/4W
R117	63-9919-86	3.9K OHM RESISTOR ±2% FILM	1/4W
RX118	63-10559-48	100 OHM RESISTOR ± 5% FAILSAFE	1/4W
RX121	63-10559-24	10 OHM RESISTOR ± 5% FAILSAFE	1/4W
R122	63-9921-46	82 OHM RESISTOR ± 5% FILM	1/4W
RX123	63-10559-48	100 OHM RESISTOR ± 5% FAILSAFE	1/4W
RX124	63-10559-68	680 OHM RESISTOR ± 5% FAILSAFE	1/4 W
			1/4W
R126	63-10184-20	100K OHM RESISTOR ±10% CARBON COMP	1/4W
RX128	63-10585	1 OHM RESISTOR ± 5% FAILSAFE	1/2W
R129	63-8797	1K OHM RESISTOR ±5% FILM	1/4W
R201		330 OHM RESISTOR ±5% CARBON COMP	1/2W
R202		16 OHM RESISTOR ± 5% CARBON COMP	1/2W
R203	REFERENCE	2.2KOHM RESISTOR ±10% CARBON COMP	1/2W
R204	ONLY	10 K OHM RESISTOR ±10% CARBON COMP	1/2W

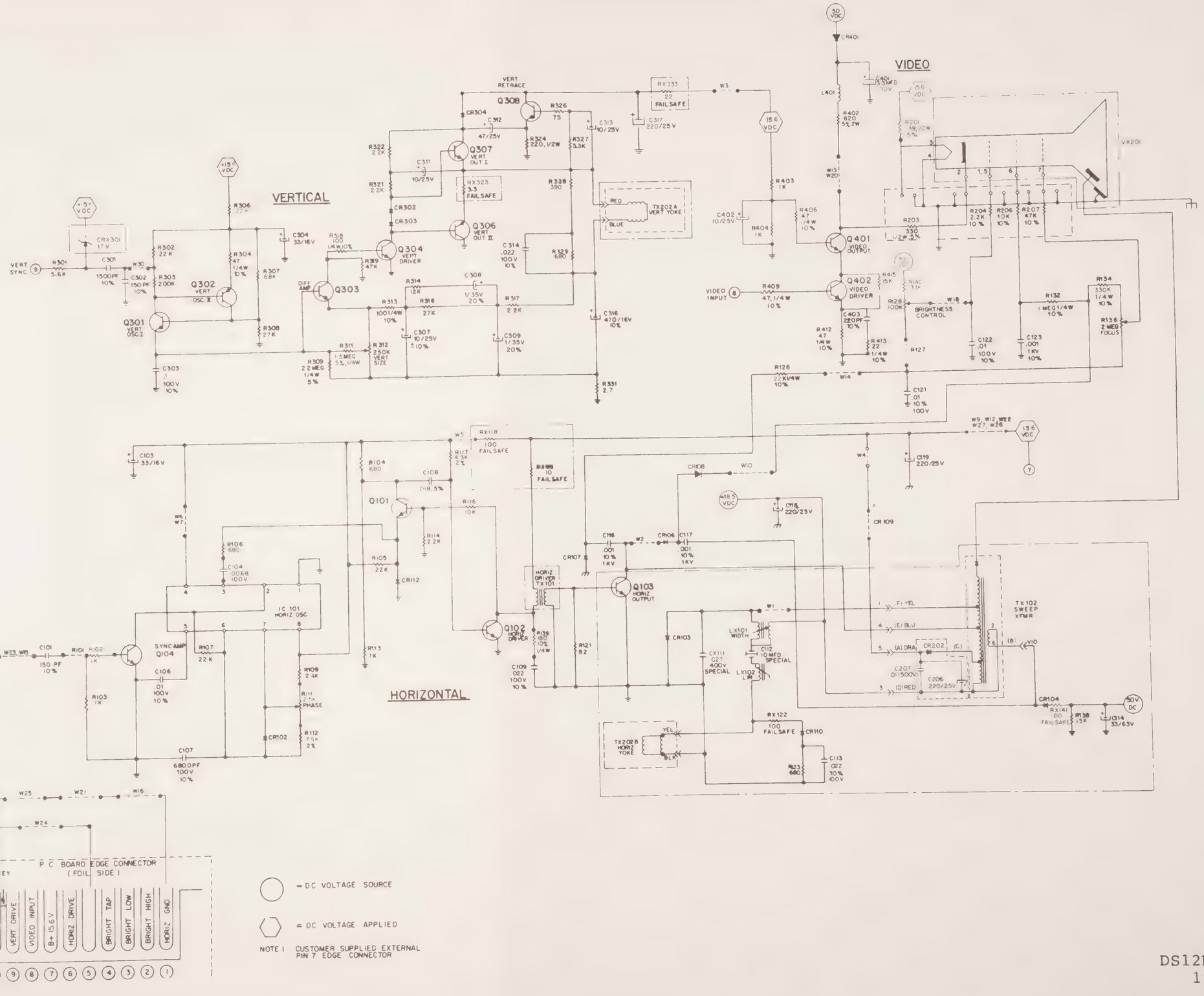
ITEM NO.	PART NO.	DESCRIPTION	
R205		47K OHM RESISTOR ±10% CARBON COMP	1/2W
R301	63-9922-27	200 K OHM RESISTOR ±5% FILM	1/4W
R302	63-9921-92	6.8 K OHM RESISTOR ± 5% FILM	1/4W
R303	63-9922-04	22K OHM RESISTOR ± 5% FILM	1/4W
R304	63-9921-95	9.1 K OHM RESISTOR ±5% FILM	1/4W
R305	63-9922-10	39K OHM RESISTOR ± 5% FILM	1/4W
R306	63-9921-40	47 OHM RESISTOR ± 5% FILM	1/4W
RX307	63-10559-36	33 OHM RESISTOR ± 5% FAILSAFE	1/4W
R308	63-9922-42	820K OHM RESISTOR ± 5% FILM	1/4W
R309	63-10651-13	CONTROL 250K OHM VERT. SIZE	
R310	63-9924-48	1.5 MEG OHM RESISTOR ± 10% FILM	1/4W
R311	63-9922-22	120 K OHM RESISTOR ± 5% FILM	1/4W
R312	63-9922-06	27K OHM RESISTOR ± 5% FILM	1/4W
R313	63-9922-10	39K OHM RESISTOR ± 5% FILM	1/4W
R314	63-9921-78	1.8 K OHM RESISTOR ± 5% FILM	1/4W
R315	63-9922	15 K OHM RESISTOR ± 5% FILM	1/4W
R316	63-9921-72	1K OHM RESISTOR ±5% FILM	1/4W
R317	63-7816	5.6 K OHM RESISTOR ± 5% CARBON COMP	1/2W
R318			
RX319	63-10565-56	220 OHM RESISTOR ± 5% FAILSAFE	1/2W
R320	63-9922-04	22K OHM RESISTOR ± 5% FILM	1/4W
R321	63-9921-45	75 OHM RESISTOR ± 5% FILM	1/4W
R322	63-9921-84	3.3K OHM RESISTOR ± 5% FILM	1/4W
R323	63-9921-73	1.1K OHM RESISTOR ±5% FILM	1/4W
R324	63-9921-44	68 OHM RESISTOR ±5% FILM	1/4W
R325	63-9921-10	2.7 OHM RESISTOR ±5% FILM	1/4W
R402	63-9921-72	1K OHM RESISTOR ±5% FILM	1/4W
R403	63-9921-72	1K OHM RESISTOR ± 5% FILM	1/4W
R404	63-9921-40	47 OHM RESISTOR ± 5% FILM	1/4 W
R405	63-8821	12K OHM RESISTOR ± 5% FILM	1/4W
R406	63-9921-32	22 OHM RESISTOR ± 5% FILM	1/4W
R407	63+10371-70	820 OHM RESISTOR ± 5% FILM	2W
R408	63-9921-40	47 OHM RESISTOR ± 5% FILM	1/4W
R411	63-9922-	15K OHM RESISTOR ±5% FILM	1/4W
R412			
R413	63-9922-04	15K OHM RESISTOR ±5% FILM	1/4W
R415	63-10812-01	CONTROL 2 MEG OHM FOCUS	
R416	63-9922-16	68K OHM RESISTOR ±5% FILM	1/4W
R417	63-9922-40	680K OHM RESISTOR ±5% FILM	1/4W
R418	63-9922	15K OHM RESISTOR ±5% FILM	1/4W
L101	20-3906	COIL,RCF LINEARITY	
L102	20-3892	COIL, RCF TUNABLE WIDTH	
L401	20-3867-10C	COIL, RCF 6.8 uh	
TX101	95-3136-03	TRANSFORMER HORIZ DRIVER	
TX201	95-3395-01	H.V. SWEEP TRANSFORMER	
TX202	95-3387-02	DEFLECTION YOKE	
CR101	103-142-01	DIODE	
CR102	103-142-01	DIODE	
CR103	103-142-01	DIODE	
CR104	103-295-03 A	DIODE	
CR105	103-284	DIODE	
CR106	212-76 -02	DIODE	
CR107	103-296-05A	DIODE	
CR108	212-76	DIODE	
CR109	103-142-01	DIODE	
CR304	103-142-01	DIODE	
CR305	212-76	DIODE	
CR401	212-76	DIODE	
Q101	121-875	TRANSISTOR	HORIZ. OSC.I
Q102	121-975	TRANSISTOR	HORIZ. OSC II
Q103	121-975	TRANSISTOR	HORIZ. OSC.III
Q104	121-975	TRANSISTOR	HORIZ. OSC.IV
Q105	121-819	TRANSISTOR	HORIZ DRIVER
Q106	121-1039	TRANSISTOR	HORIZ. OUTPUT
Q301	121-975	TRANSISTOR	VERT. OSC. I
Q302	121-699	TRANSISTOR	VERT. OSC. II
Q303	121-699	TRANSISTOR	VERT. AMP. I
Q304	121-975	TRANSISTOR	VERT. AMP. II
Q305	121-972	TRANSISTOR	VERT. DRIVER
Q306	121-819	TRANSISTOR	VERT. OUTPUT I
Q307	121-873	TRANSISTOR	VERT. OUTPUT II
Q308	121-819	TRANSISTOR	VERT. RETRACE
Q401	121-1058	TRANSISTOR 121-1034 ALT.	VIDEO OUTPUT
Q402	121-895	TRANSISTOR	VIDEO DRIVER
YX201	100-684	12" CRT	
OR	100-684-02	12" CRT	

ITEM NUMBER	PART NUMBER	DESCRIPTION
C101	22-7742	150 PFD CAPACITOR 10% TUBULAR 50V
C102		
C103	22-7707-07A	33 MFD CAPACITOR +50-10% ELEC. 16V
C104	22-7773-10	.0068 MFD CAPACITOR 5 % POLY 100V
C105		
C106	22-7774-12	.01 MFD CAPACITOR 10% POLY. 100V
C107	22-7773-10	.0068 PFD CAPACITOR 5 % POLY. 100V
C108	22-7773-15	.048 MFD CAPACITOR 5% POLY 100 V
C109	22-7774-16	.022 MFD CAPACITOR 10% POLY 100V
C110		
CX111	22-7788-05	.027 MFD CAPACITOR 5% POLY. SPECIAL 400V
C112	22-7313A	10 MFD CAPACITOR SPECIAL NON-POLARIZED
C113	22-7774-16	.022 MFD CAPACITOR ±10% POLY. 100V
C114	22-7711-07A	33 MFD CAPACITOR +50-10% ELEC. 63V
C115		
C116	22-7787	.001 MFD CAPACITOR ±10% DISC. 1KV
C117	22-7787	.001 MFD CAPACITOR ±10% DISC. 1KV
C118	22-7708-10C	220 MFD CAPACITOR +50-10% ELEC. 25V
C119	22-7708-10C	220 MFD CAPACITOR +50-10% ELEC. 25V
C120		
C121	22-7774-12	.01 MFD CAPACITOR ±10% POLY. 100V
C122	22-7774-12	.01 MFD CAPACITOR ±10% POLY. 100V
C123	22-7787	.001 MFD CAPACITOR ±10% DISC. 1KV
C124		
C125		
C126		
C127		
C128		
C206		
C207		
C301	22-7742-12	1500 PFD CAPACITOR ±10% TUBULAR 50V
C302	22-7742	150 PFD CAPACITOR ±10% TUBULAR 50V
C303	22-7773-24	.1 MFD CAPACITOR ± 5% POLY 100V
C304	22-7707-07A	33 MFD CAPACITOR +50-10% ELEC. 16V
C305		
C306		
C307	22-7389-14C	10 MFD CAPACITOR ±10% ELEC. 25V
C308	22-7713-02A	1 MFD CAPACITOR ±20% ELEC. 35V
C309	22-7713-02A	1 MFD CAPACITOR ±20% ELEC. 35V
C310		
C311	22-7708-05A	10 MFD CAPACITOR +50-10% ELEC. 25V
C312	22-7708-08A	47 MFD CAPACITOR +50-10% ELEC. 25V
C313	22-7708-05A	10 MFD CAPACITOR +50-10% ELEC. 25V
C314	22-7774-16	.022 MFD CAPACITOR ±10% POLY. 100V
C315		
C316	22-7579-12B	470 MFD CAPACITOR ±10% ELEC. 16V
C317	22-7708-10C	220 MFD CAPACITOR ±50%-10% ELEC. 25V
C318		
C319		
C320		
C321		
C401	22-7712-03A	3.3 MFD CAPACITOR ±10% ELEC 100V
C402	22 7708-05A	10 MFD CAPACITOR +50-10% ELEC 25 V
C403	22-7742-02	220 PFD CAPACITOR ±10% TUBULAR 50 V
C404		
C405		
C406		
C407		
C408		
R101		
R102	63-10235-72	1K OHM RESISTOR ± 5% FILM 1/4W
R103	63-10235-72	1K OHM RESITOR ± 5% FILM 1/4W
R104	63-10235-68	680 OHM RESISTOR ±5% FILM 1/4 W
R105	63-10236-04	22K OHM RESISTOR ±5% FILM 1/4W
R106	63-10235 68	680 OHM RESISTOR ·5% FILM 1/4W
R107	63 10236-04	22K OHM RESISTOR ·5% FILM 1/4W
R108		
R109	63-10235-81	2.4K OHM RESISTOR ±5% FILM 1/4W
R110		
R111	63-10857-09	2.5 K OHM CONTROL PHASE
R112	63-10233-93	7.5K OHM RESISTOR ·2% FILM 1/4W
R113	63-10235-72	1K OHM RESISTOR ±5% FILM 1/4W
R114	63-10235-80	2K OHM RESISTOR ±5% FILM 1/4 W
R115		
R116	63 10235-96	10 K OHM RESISTOR ±5% FILM 1/4 W
R117	63-10233-81	6.3K OHM RESISTOR ·2% FILM 1/4 W
RX118	63-10559-48	100 OHM RESISTOR ·5% FAILSAFE 1/4W
RX119	63-10559-24	10 OHM RESISTOR ·5% FAILSAFE 1/4W
R120		
R121	63 10235 46	82 OHM RESISTOR ·5% FILM 1/4W
RX122	63-10559-48	100 OHM RESISTOR ·5% FAILSAFE 1/4W
R123	63-10235-68	680 OHM RESISTOR ±5% FILM 1/4W
R124		
R125		
R126	63-10184-04	22 K OHM RESISTOR ±10% CARBON COMP ½W
R127		
R128	63-10857-17	100K OHM CONTROL BRIGHTNESS
R129		
R130		
R131		
R132	63-10184-44	1.0 MEG OHM RESISTOR ·10% CARBON COMP ½W
R133		
R134	63 10184-32	330K OHM RESISTOR ·10% CARBON COMP. ½W
R135		
R136	63-10857-24	CONTROL FOCUS 2 MEG OHM
R137		
R138	63-10236	15K OHM RESISTOR ·5 % FILM 1/4W
R139	63-10183-54	180 OHM RESISTOR ·10% CARBON COMP ½W
R140	63-10235-08	33K OHM RESISTOR ± 5Y FILM 1/4W
RX141	63-10559-48	100 OHM RESISTOR ± 5% FAILSAFE 1/4 W
R142		
R143		
R144		
R145		
R201	63-7725	39 OHM RESISTOR 5% CARBON 1/4W
R202		
R203	REFERENCE	330 OHM RESISTOR 5% C C 1/2W
R204	REFERENCE	2.2 K OHM RESISTOR ± 10 % C C 1/2W
R205		
R206	REFERENCE	10 K OHM RESISTOR ±10% C C 1/2W
R207	REFERENCE	47K OHM RESISTOR ±10% C C 1/2 W

ITEM NUMBER	PART NUMBER	DESCRIPTION
R301	63-10235-90	5.6K OHM RESISTOR 5% FILM ¼W
R302	63-10236-04	22K OHM RESISTOR 5% FILM ¼W
R303	63-10236-27	200K OHM RESISTOR 5% FILM ¼W
R304	63-10183-40	47 OHM RESISTOR ±10% CARBON COMP. ¼W
R305		
R306	63 10236-04	22K OHM RESISTOR ±5% FILM ¼W
R307	63-10235-92	6.8K OHM RESISTOR ±5% FILM ¼W
R308	63-10236-06	27K OHM RESISTOR ±5% FILM ¼W
R309	63-10182-52	2.2 MEG OHM RESISTOR ±5% CARBON COMP ½W
R310		
R311	63-10182-48	1.5 MEG OHM RESISTOR ±5% CARBON COMP ½W
R312	63-10857-20	CONTROL VERT. SIZE 250K ohm
R313	63-10183-48	100 OHM RESISTOR ±10% CARBON COMP. ½W
R314	63-10235-98	12K OHM RESISTOR ±5% FILM. ¼W
R315		
R316	63-10236-06	27K OHM RESISTOR ±5% FILM ¼W
R317	63-10235-80	2.2K OHM RESISTOR ±5% FILM ¼W
R318	63-10183-48	100 OHM RESISTOR ±10% CARBON COMP. ½W
R319	63-10236-12	47K OHM RESISTOR ±5% FILM ¼W
R320		
R321	63-10235-80	2.2K OHM RESISTOR ±5% FILM ¼W
RX322	63 10235-80	2.2K OHM RESISTOR ±5% FILM ¼W
RX323	63-10559-12	3.3 OHM RESISTOR ±5% FAILSAFE ¼W
R324	63-10243-56	220 OHM RESISTOR ±5% FILM ¼W
R325		
R326	63-10235-45	75 OHM RESISTOR ±5% FILM ¼W
R327	63-10235-84	3.3K OHM RESISTOR ±5% FILM ¼W
R328	63 10235-62	390 OHM RESISTOR ±5% FILM ¼W
R329	63 10235-68	680 OHM RESISTOR ±5% FILM ¼W
R330		
R331	63 10235-10	2.7 OHM RESISTOR ±5% FILM ¼W
R332		
RX333	63-10559-32	22 OHM RESISTOR ±5% FILM 1/4W
R401		
R402	63-10836-70	820 OHM RESISTOR ±5% METAL FILM 2W
R403	63-10235-72	1 K OHM RESISTOR ±5% FILM 1/4W
R404	63-10235-72	1 K OHM RESISTOR ±5% FILM 1/4W
R405		
R406	63-10183-40	47 OHM RESISTOR ±10% CARBON COMP 1/4W
R407		
R408		
R409	63-10183-40	47 OHM RESISTOR 10% CARBON COMP ¼W
R410		
R411		
R412	63-10183-40	47 OHM RESISTOR ±10% CARBON COMP. ¼W
R413	63-10183-32	22 OHM RESISTOR ±10% CARBON COMP ¼W
R414		
R415	63-10236	15 K OHM RESISTOR ± 5 % FILM 1/4W
R416		
R417		
R418		
CR101		
CR102	103-142-01	DIODE
CR103	103-339-04A	DIODE ALT 103-316-04A
CR104	103-323-03A	DIODE
CR105		
CR106	103-323-04A	DIODE
CR107	103-285-03A	DIODE
CR108	103-323-03A	DIODE
CR109		
CR110	103-254-01	DIODE
CR111		
CR112	103-142-01	DIODE
CR113		
CR114		
CR115		
CRX301	103-279-26A	DIODE ZENER 17V 2%
CR302	103-142-01	DIODE
CR303	103-142-01	DIODE ALT. 103-316-04A
CR304	103-254-01	DIODE
CR305		
CR306		
CR307		
CR308		
CR309		
CR401	103-254-01	DIODE
LX101	20-3943-02	COIL - WIDTH
LX102	20-3906	COIL - LINEARITY
L103		
L104		
L105		
L106		
L107		
L401	20-3801-10A	COIL - 8.8 uH PEAKING - TUBULAR
L402		
L403		
L404		
L405		
L406		
Q101	121-975A	TRANSISTOR HORIZ OSC
Q102	121-1040A	TRANSISTOR HORIZ DRIVER
Q103	121-1070	TRANSISTOR HORIZ OUTPUT
Q104	121-975A	TRANSISTOR SYNC AMP
Q105		
Q106		
Q107		
Q109		
Q110		

ITEM NUMBER	PART NUMBER	DESCRIPTION
Q301	121-975A	TRANSISTOR VERTICAL OSC I
Q302	121-699A	TRANSISTOR VERTICAL OSC II
Q303	121-699A	TRANSISTOR DIFF AMP
Q304	121-1040A	TRANSISTOR VERTICAL DRIVER
Q305		
Q306	121-1036	TRANSISTOR VERTICAL OUT II
Q307	121-1035	TRANSISTOR VERTICAL OUT I
Q308	121-1040A	TRANSISTOR VERTICAL RETRACE
Q309		
Q310		
Q311		
Q312		
Q313		
Q401	121-1058	TRANSISTOR VIDEO OUTPUT
Q402	121-895A	TRANSISTOR VIDEO DRIVER
TX101	95-3138-03	TRANSFORMER - HORIZ. DRIVER
TX102	95-3457	TRANSFORMER - H.V. SWEEP OFF BOARD
TY202	95-3397-02	DEFLECTION YOKE - 90° OFF BOARD
IC101	221-217	INTEGRATED CIRCUIT
VX201	100-724-01	C.R.T

DS12NK150 SERIES
18.6, 19.2 KHZ



DS12NK150 SERIES
18.6, 19.2 KHZ

7. SCHEMATIC DIAGRAMS

REVISION STATUS				
REV	ZONE	DESCRIPTION	DATE	APPR
FA		REV PER ECN 463	1/12/82	

J1
4
3
1
5
6
7

C14 CR1 6A, 100 PIV .01V
C13 CR2 6A, 100 PIV .01V
CR3 6A, 100 PIV .01V C15
CR4 6A, 100 PIV .01V C12
C10 CR5 IN5401 .01V
C9 CR6 IN5401 .01V
CR7 IN5401 .01V C11
CR8 IN5401 .01V C16

RAW +5
J2-φ
J3-φ

C1 10,000 mf 25V
C17 470 Pf
C3 4700 mf 50V
C4 470 mf 50V
C5 22 mf 16V
C8 22 mf 16V
C2 22 mf 16V
C7 .0022 uf

R1 1.8 Ω 2WATT
R2 .36 Ω, 2 WATT
R3 .36 Ω, 2 WATT
R4 2.7 Ω 2WATT
R5 0.56 Ω 2watt
R7 1K 1/4 W
R8 1K, 1/4W

Q6 TIP34
Q5 2N4901 ①
Q1 TIP34
Q2 2N4901 ①
Q3 TIP34
Q4 TIP34 ②

VR1 7805 ①
VR2 7815 ③
VR3 7812
VR4 7905 ⑤
IN OUT

CR9 IN914

1 2 J2
1 2 J3
8 9 J2
8 9 J3
4 5 J2
4 5 J3
J2-7
J3-7
J2-6
J2-6
CHAS. GRD.

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TOLERANCES: Except as noted		DRAWN	12-9-81
INCHES/MM		CHECKED	1/12/82
.X = /		APPR.	1/1/82
.XX = /		APPR.	
.XXX = /			
FRACT. =			
ANGLE =			
Material		SIGNATURE	DATE
Finish			

VISUAL
Visual Technology Incorporated
Railroad Avenue, Dundee Park, Andover, Ma. 01810

REV FA

TITLE: SCHEMATIC (POWER SUPPLY)

SIZE: C | SCALE: NONE

UNIT NO. PS005-001

Model No. | Next Assy. | SHEET 1 OF 1

VISUAL FORM VF001-013

REVISION STATUS				
REV	ZONE	DESCRIPTION	DATE	APPR
A	-	RELEASED		

22-00950-003

Z4

Z6

Z10

Z7

Z8

Z1 = 22-07805-605
48-00035-007

UNUSED GATES

Z3 7437 1 PLC

<1> NOT NORMALLY INSTALLED

<2> ON-05X ASSY INSTALL
20-08035-000 AT Z6
DELETE ETCH TIE E3 TO E4

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Material:	TOLERANCES: Except as noted	DRAWN K Payne	11/16/82	VISUAL Visual Technology Incorporated Railroad Avenue, Dundee Park, Andover, Ma. 01810
Finish:	INCHES/MM .X = .XX = .XXX = FRACT. = ANGLE =	CHECKED		REV A
		APPR.		TITLE: SCHEMATIC KEYBOARD
		APPR.		SIZE C SCALE: NONE
		SIGNATURE	DATE	UNIT NO. K5005-015
				Model No. V500/550 Next Assy. KA005-A01 SHEET 1 OF 1

VISUAL FORM VF001-013

REVISION STATUS				
REV	ZONE	DESCRIPTION	DATE	APPR
BA		PCL [illegible] 360	2/14/82	SAB
EE		REV PER 00380		

REVISION STATUS				
REV	ZONE	DESCRIPTION	DATE	APPR
EL		REV PER 430	5/12/82	[illegible]
BD		REV PER 416	[illegible]	[illegible]
BE		REV PER 366	5/12/82	[illegible]
BF		REV PER 430	5/12/82	[illegible]

+5V
RP2
4.7K
CINT
VIDIPT
MREQ
IOREQ
RD
WR
VREFA
RESET
M1
RFSH
NMI-
HALT
BUSAK
WAIT-
BUSRQ
U40
Z80
PCLOCK
AB0
AB1
AB2
AB3
AB4
AB5
AB6
AB7
AB8
AB9
AB10
AB11
AB12
AB13
AB14
AB15
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7

+5V
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
RESET
RD
DWR
SPIO
AB0
AB1
U51
8255
PORT A
PORT B
PORT C
BRD0
BRD1
BRD2
BRD3
BRD4
PREV
BLINKF
ACRAM
RDE
LDE
ACTS
TXE
EGKID
SYNC
PDSR
DSR
ODEVFL
PIPT
VIDIPT

DWR
WR
PCLOCK
U73
74LS74
VREFA
VREFA

WR
AB6
U77
74LS139
SVDWR
SVSRD
SVAWR
SVARD

AB14
AB13
AB11
AB12
AB15
MREQ
RFSH
U37
74LS138
ROM0
ROM1
ROM2
RAMSEL

+5V
RP3
4.7K
DB7
DB1
DB2
DB3
DB4
DB5
DB6

RXCLK
TXT
RXCLK
RXT
SYNC
U54
74LS257
TXC
RXC

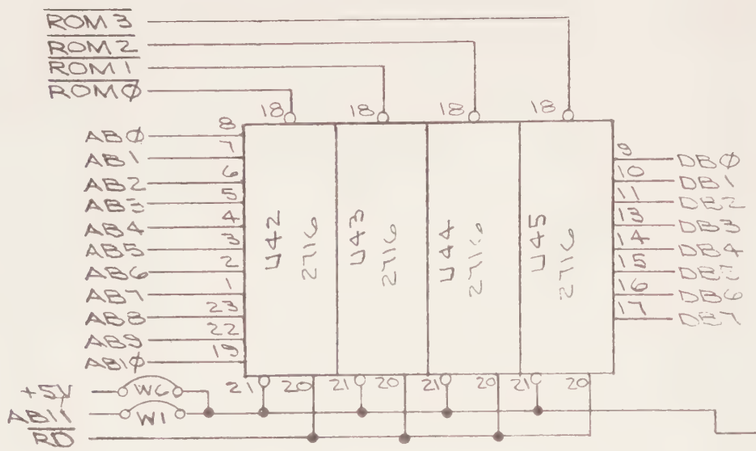
AB4
AB5
AB6
AB7
IOREQ
M1
U62
74LS138
SBRG0
SPIO
SPUSART
SMPSC
SBRG1
SVTAC

RD
WR
LS32
U61
SGDCR
SGDCW

ACRAM
U38
74LS138
ROM3
PN3643
Q7
CRAMS
RD
WR
LS00
U36
+5V
Q6
PN3644
R44
180R
R43
1K
R41
2.2K
R42
2.2K

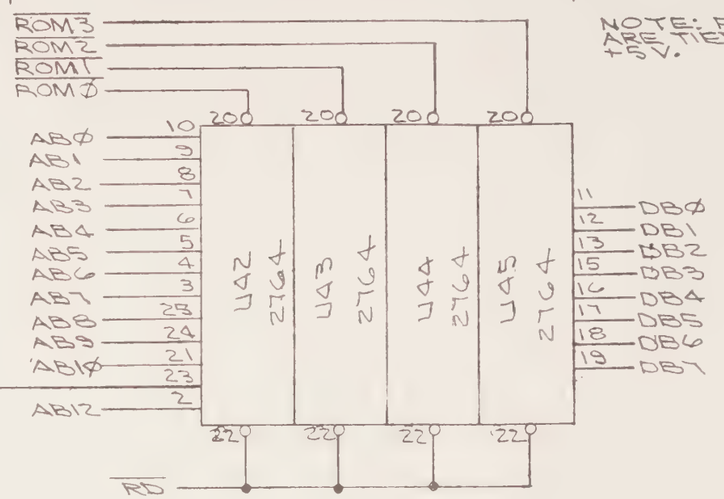
TOLERANCES Except as noted INCHES-MM	DRAWN	VISUAL Visual Technology Incorporated Railroad Avenue Dundee Park Andover Ma (01810)	REV F	
X = XX = XXX = FRACT = ANGLE =	CHECKED 1/22/81	TITLE SCHEMATIC PROCESSOR & SELECTS	SIZE D	SCALE NONE
Material	APPR 12/9/81		UNIT NO P5016-001	
Finish	APPR 12/9/81	Model No. V-[illegible]00	Next Assy	SHEET 1 OF 3
	SIGNATURE DATE			

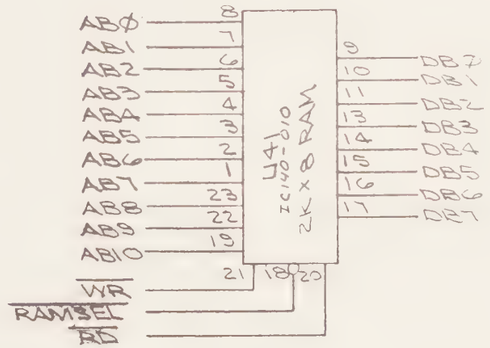
REVISION STATUS				
REV	ZONE	DESCRIPTION	DATE	APPR
BF		SEE SHEET 1	12/9/81	GB

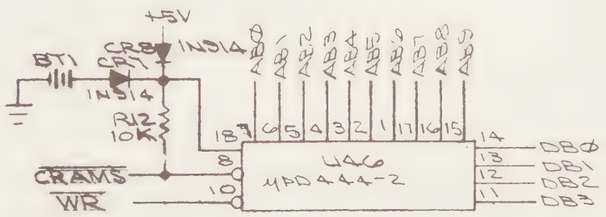


OPTIONAL PROMS

NOTE: PINS 1, 26, 27 & 28 ARE TIED TOGETHER & TO +5V.







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Material:

Finish:

TOLERANCES: Except as noted
INCHES/MM
.X = /
.XX = /
.XXX = /
FRACT. =
ANGLE =

DRAWN	W.E. Barnes	5/28/81
CHECKED		
APPR.	SAB	12/9/81
APPR.	B Lough	12/8/81
SIGNATURE		DATE

VISUAL
Visual Technology Incorporated
Railroad Avenue, Dundee Park, Andover, Ma. 01810

REV. BF

TITLE: SCHEMATIC RAM & ROM & [illegible]

SIZE C | SCALE: NONE

UNIT NO 950[illegible]

Model No. V-5[illegible] | Next Assy. | SHEET 2

VISUAL FORM 4P001-013

REVISION STATUS				
REV	ZONE	DESCRIPTION	DATE	APPR
BA		ECR SHEET 1	8/4/81	CB

MODEM PORT

+5V

RP1 RES PACK 4.7K

DSR
CD
RXT
TXT
CLOOP

1489

C2 390pf, C1 390 Pf, C4 390 Pf, C9 390 Pf, C5 390 Pf, C3 390 Pf

TXE
TXD

RP2 2

U57 7426

GTXD

ACTS

U64 74LS51

74LS04

CTS

ROE
LDE

U64 74LS51

RXD

TXD

SCCD

C8 390 Pf

+5V

R6 150Ω

U68B MCT-2

Q3 MPSA55

MPSA06

Q2

C18 270pf

RB 390Ω

CR3

MCL1301

R7 6BK

GTXD

+12V

R9 510

CR2 IN914

25

+12V

RA 510Ω

EIA

18

CR1 IN914

Q1 MPSA06

R3 36Ω

17

R2 2.2K

68A MCT-2

R5 150K

+12V

R1 10K

CLOOP

+12V -12V

CR5 IN914

CR4 IN914

MODEM PORT

RTS
DRT
SCRTS

U56 1488

C17 390 Pf, C15 390 Pf, C16 390 Pf

C19 390 Pf

1488

AUX PORT

PTXD
PDTR
PRXD
PBUSY
PDSR

U79 1488

C7 390 Pf
C11 390 Pf
C12 390 Pf
C13 390 Pf

RPD 4.7K

+5V

R54 4.7K

C29 390PF

1489

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Material	
Finish	

TOLERANCES Except as noted
INCHES MM
X =
XX =
XXX =
FRACT
ANGLE =

DRAWN		8/3/81
CHECKED		
APPR		8/4/81
APPR		10/5/81
SIGNATURE	DATE	

VISUAL
Visual Technology Incorporated
Railroad Avenue Dundee Park Andover, Ma 01810

REV. BF

TITLE: SCHEMATIC EIA

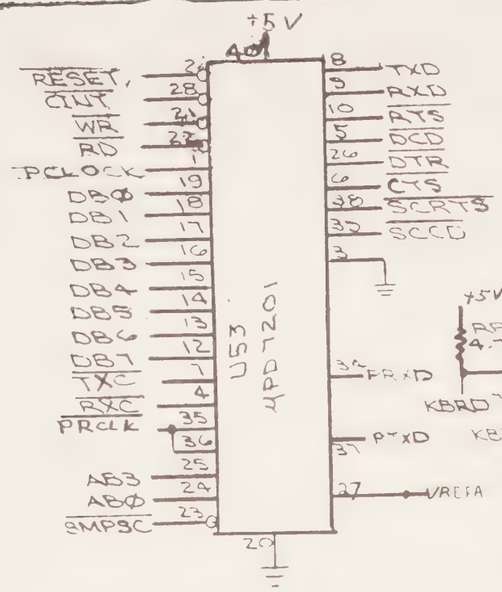
SIZE C | SCALE: NONE

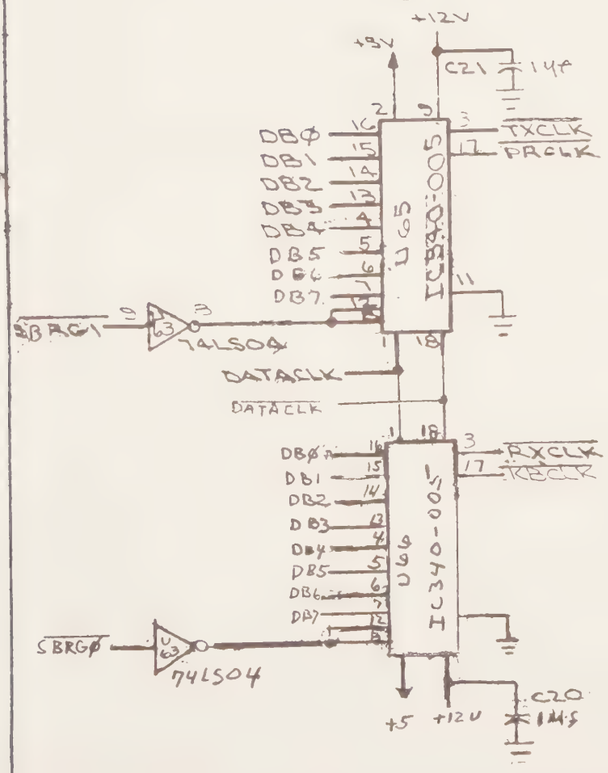
UNIT NO PS016-001

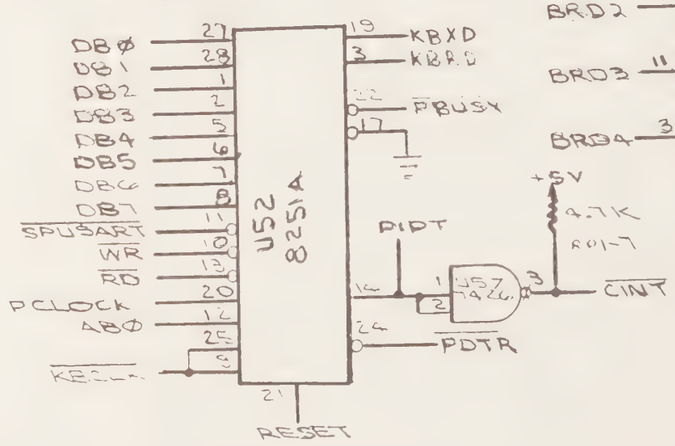
Model No V-500 | Next Assy

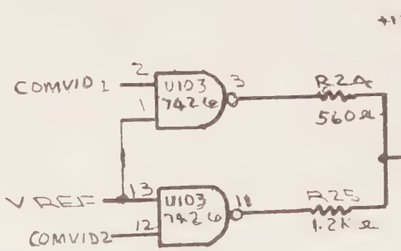
SHEET 3 OF 3

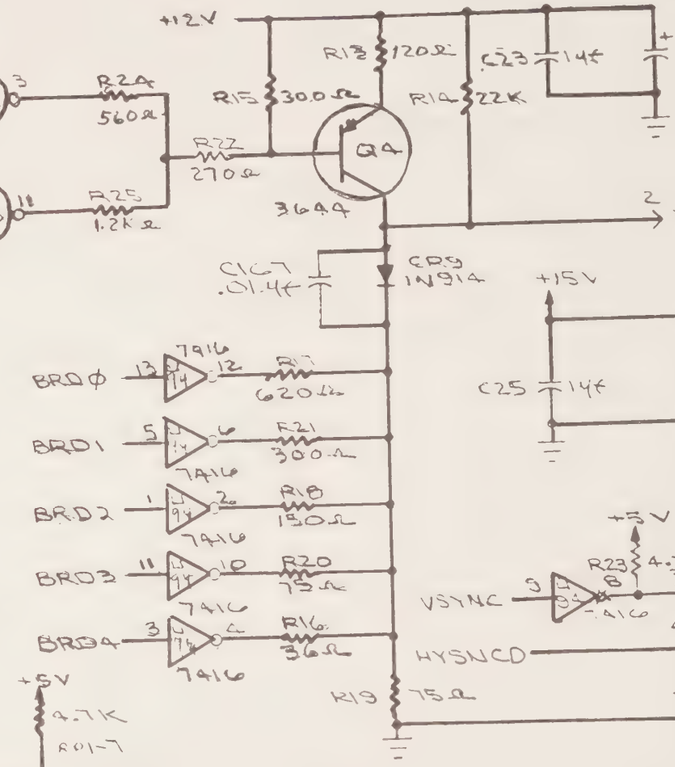
REVISION STATUS				
REV	ZONE	DESCRIPTION	DATE	APPR
6F		SEE SHEET 1	12/16/81	











JUMPER LIST

JUMPER	IN/OUT	JUMPER	IN/OUT	JUMPER	IN/OUT	JUMPER	IN/OUT	JUMPER	IN/OUT	JUMPER	IN/OUT	DEVICE
W1	O	W2	I	W3	I	W4	O	W5	O	W6	I	2K x 8
W1	I	W2	I	W3	O	W4	O	W5	I	W6	O	4K x 8
W1	I	W2	O	W3	O	W4	I	W5	I	W6	O	8K x 8

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TOLERANCES: Except as noted
INCHES/MM
.X ±
.XX ±
.XXX ±
TRACK ±
ANGLE ±

DRAWN
CHECKED
APPD
MGR
ENGINEERING

VISUAL
Visual Technology Incorporated
Railroad Avenue, Dundee Park, Andover, MA 01810

TITLE: SCHEMATIC
VIDEO & DMA CONTROL

SIZE: C
DWG NO: 6
SCALE:

REVISION STATUS				
REV	ZONE	DESCRIPTION	DATE	APPR
BF		SEE SHEET 1	12/6/	

+5V
U83A
34.8456MHZ
OSC
(N.C.)
VREFA
U84 74F74
DCLK
+5V
U74
74LS93
+5V
R111 330Ω
U63
74LS04
PCLOCK
VREFA
U84 74F74
VREFA
VREFA
VREFA
VREFA
VREFA
74F04
U75
VREFA
74F04
U75
74F04
DADD3
DADD4
DADD5
DADD6
DADD12
U85
74S174
ODEFL
VREF
+5V
BLANK
U75
74F04
RD
WR
SVTAC
ABO
AB1
AB2
DBO
DB1
DB2
DB3
DB4
DB5
DB6
DB7
CCLK
BLANK
VSYNC
HSYNC
CURSOR
U86
2672
DADDØ
DADD1
DADD2
DADD3
DADD4
DADD5
DADD6
DADD7
DADD8
DADD9
DADDIØ
DADD11
DADD13
VBWR
VBLANK
VBWR
VDIFF
DADD12
VDBO
VDB1
VDB2
VDB3
VDB4
VDB5
VDB6
VDB7
VREFA
U98
LS273
74F04
CCLK
2732
U97
U105
LS08
U105
LS08
U96
2673
CCLK
DCLK
BLANK
BLINKA
ULATT
BOLDAT
RV
HSYNC
VREF A
BLANK
DADDIØ
BLINK
DADD13
+5V
3.3V
CR10
IN4728
C26
4.7 uf
U76
74LS86
RVIDAT
CURSOR
VREFA
U95
19F74
TTLVID2
DCLK
VREFA
U95
19F74
TTLVID1
VREF
+5V
GSRD
DCLK
VREFA
U70
F174
CPREV
TTLVID2
U70
F174
LS86
U80
COMVID2
U70
F174
TTLVID1
LS86
U80
COMVID1
U70
F174
Y1
1.8432MHZ
C28
22PF
R26
11.2K
C90
22PF
74LS04
74LS04
74LS04
74LS04
74LS04
C168
22pf
74LS04
DATACLK
DATACLK

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Material

Finish

TOLERANCES
Except as noted
INCHES/MM
X = /
XX = /
XXX = /
FRACT =
ANGLE =

DRAWN		
CHECKED		
APPR	12/4/5	
APPR	12/4/5	
SIGNATURE		DATE

VISUAL
Visual Technology Incorporated
Railroad Avenue, Dundee Park, Andover, Ma. 01810

REV BF

TITLE: SCHEMATIC VIDEO 1 CLOCK LOGIC

SIZE NONE

SCALE:

UNIT NO. PS016-0.1

Model No. V-500

Next Assy.

SHEET 5 OF 9

REVISION STATUS				
REV	ZONE	DESCRIPTION	DATE	APPR
E F		SEE SHEET 1		

VWR → 74LS04 → VRD

U99 2K x 8 RAM
U100 2K x 8 RAM
DADD0 DADD1 DADD2 DADD3 DADD4 DADD5 DADD6 DADD7 DADD8 DADD9 DADD10 VWR VRD
VDB0 VDB1 VDB2 VDB3 VDB4 VDB5 VDB6 VDB7

U77 74LS139
DADD11 DADD12 VRAME

U102 2K x 8 RAM
U101 2K x 8 RAM
DADD0 DADD1 DADD2 DADD3 DADD4 DADD5 DADD6 DADD7 DADD8 DADD9 DADD10 VWR VRD
BLINKA ULATT BOLDAT RVIDAT SPAT1 SPAT2 GREAT

+5V
RP4 4.7K RES PACK

U104 74LS04
BLANKA BLINKA ULATT BOLDAT RVIDAT

SVDWR VBWR
U87 74LS374
U85 74LS374
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7
VDB0 VDB1 VDB2 VDB3 VDB4 VDB5 VDB6 VDB7

SVDRD SVARD
VWR
U89 74LS374
U90 74LS374
SVAWR SVAWR

+5V
CR6 IN914
R10 10K
C6 22µf 16V
U49 74LS04
RESET
RP4-4 +5V
RESET

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Material
Finish.

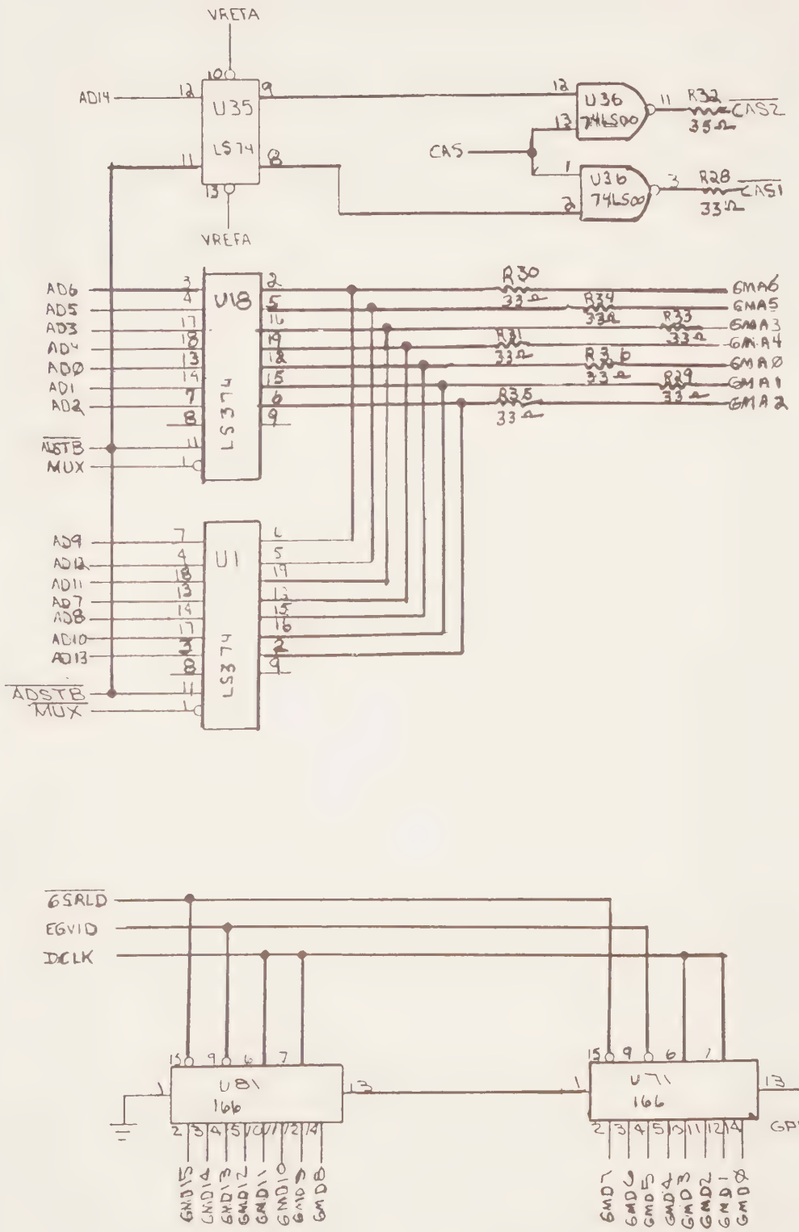
TOLERANCES: Except as noted
INCHES/MM
.X = /
.XX = /
.XXX = /
FRACT =
ANGLE =

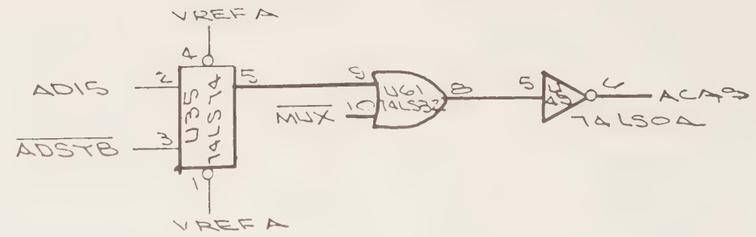
DRAWN
CHECKED
APPR BAD 12/1/81
APPR B. Engh 12/9/81
SIGNATURE DATE

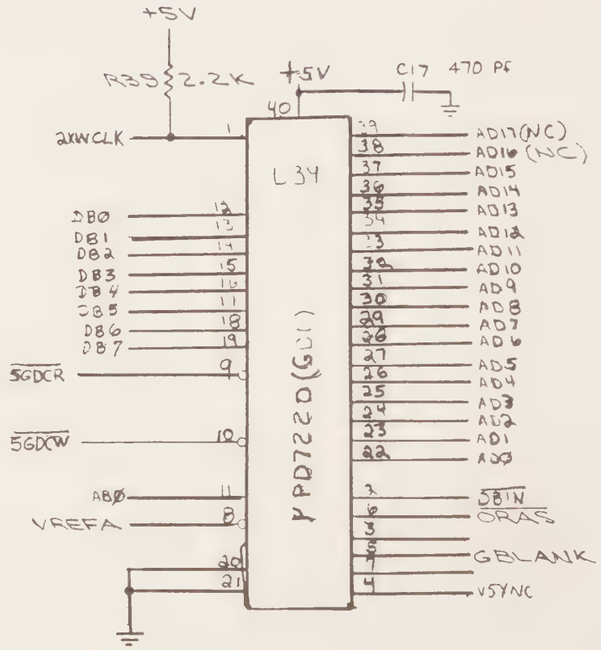
VISUAL
Visual Technology Incorporated
Raitroad Avenue Dundee Park, Andover, Ma. 01810

TITLE: SCHEMATIC VIDEO RAM & ATTRIBUTE LOGIC
SIZE: C
SCALE: NONE
UNIT NO: PS016-001
Model No: V-500
Next Assy
SHEET 6 OF 9
REV D F

REVISION STATUS				
REV	ZONE	DESCRIPTION	DATE	APPR
B5		SEE SHEET 1		







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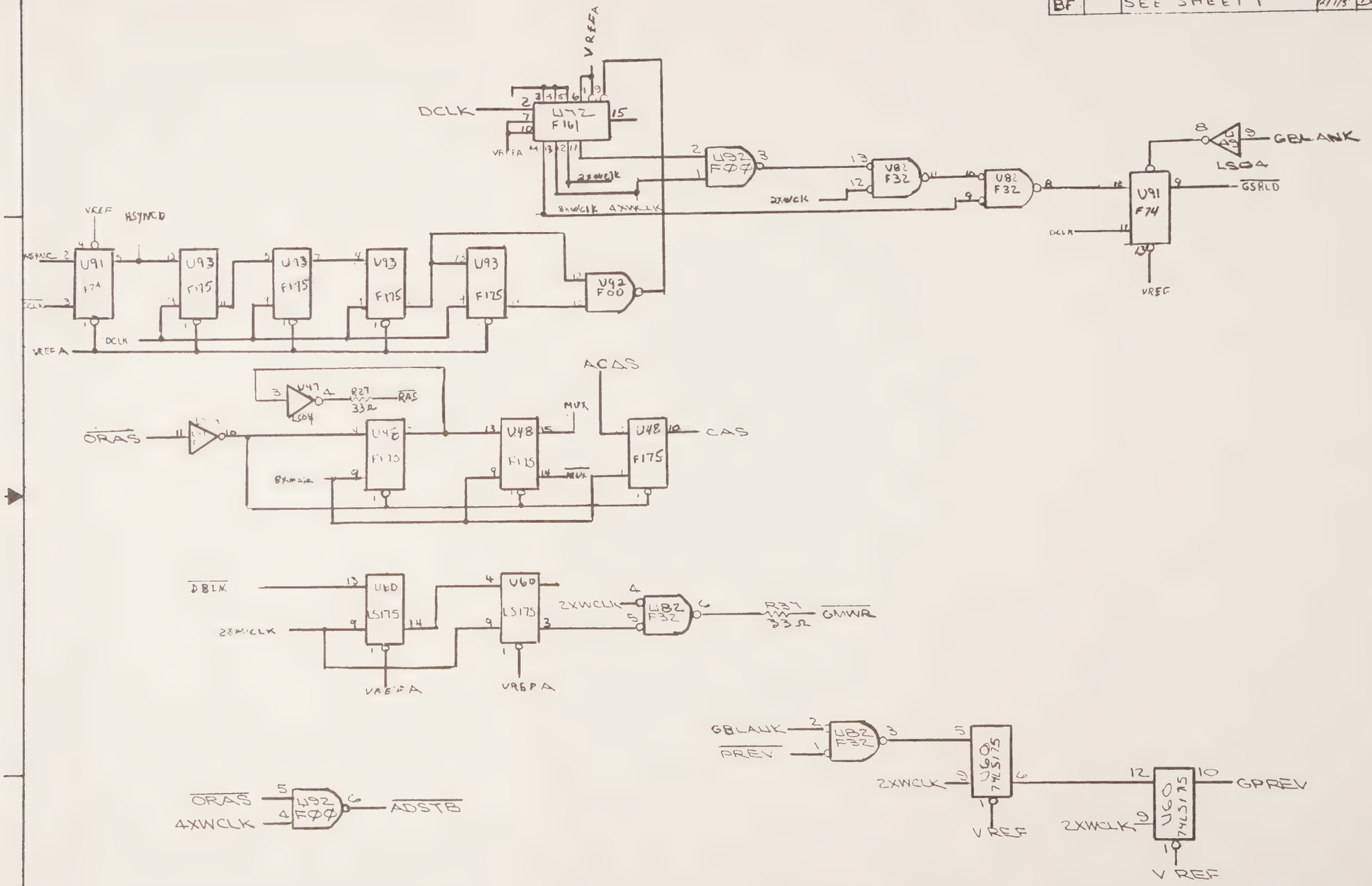
Material			TITLE: SCHEMATIC GRAPHICS CONTROL	SIZE	SCALE:
Finish				UNIT NO. PSD16-001	
			Model No. V5DD	Next Assy.	SHEET 7 OF 9

REVISION STATUS				
REV	ZONE	DESCRIPTION	DATE	APPR
BF		SEE SHEET 1	12/9/5	BH



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Material		CHECKED		TITLE: GRAPHIC VIDEO TIMING
Finish		APPR.	12/91	SIZE: C SCALE:
		APPR.	12/9/91	UNIT NO.
		SIGNATURE	DATE	Model No. / Next Assy. / SHEET 8 OF 9

REV. B.F.

REVISION STATUS				
REV	ZONE	DESCRIPTION	DATE	APPR
BF		SEE SHEET 1	9/9/81	BB

-12V — VR1 — -5V

R38 470

CAS1, GMWR, RAS, GMA0, GMA1, GMA2, GMA3, GMA4, GMA5, GMA6, CAS2, GMWR, RAS, GMA0, GMA1, GMA2, GMA3, GMA4, GMA5, GMA6

U17 U16 U15 U14 U13 U12 U11 U10 4116

U24 U23 U22 U21 U30 U29 U28 U27 4116

AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7

GM0 GM1 GM2 GM3 GM4 GM5 GM6 GM7

U47 74LS244

AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7

AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15

GM8 GM9 GM10 GM11 GM12 GM13 GM14 GM15

U59 74LS244

AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15

DBIN

CAS1, GMWR, RAS, GMA0, GMA1, GMA2, GMA3, GMA4, GMA5, GMA6, CAS2, GMWR, RAS, GMA0, GMA1, GMA2, GMA3, GMA4, GMA5, GMA6

U32 U31 U40 U39 U38 U37 U36 U35 4116

U19 U20 U21 U22 U23 U24 U25 U26 4116

VISUAL FORM VF001-013

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Material:

Finish:

TOLERANCES: Except as noted
INCHES/MM
.X = /
.XX = /
.XXX = /
FRACT. =
ANGLE =

DRAWN	E Bailey	9-25-81
CHECKED		
APPR.	BB	12/5/81
APPR.	E Langlois	12/9/81
SIGNATURE		DATE

VISUAL
Visual Technology Incorporated
Railroad Avenue, Dundee Park, Andover, Ma. 01810

REV. BF

TITLE: SCHEMATIC GRAPHICS RAM

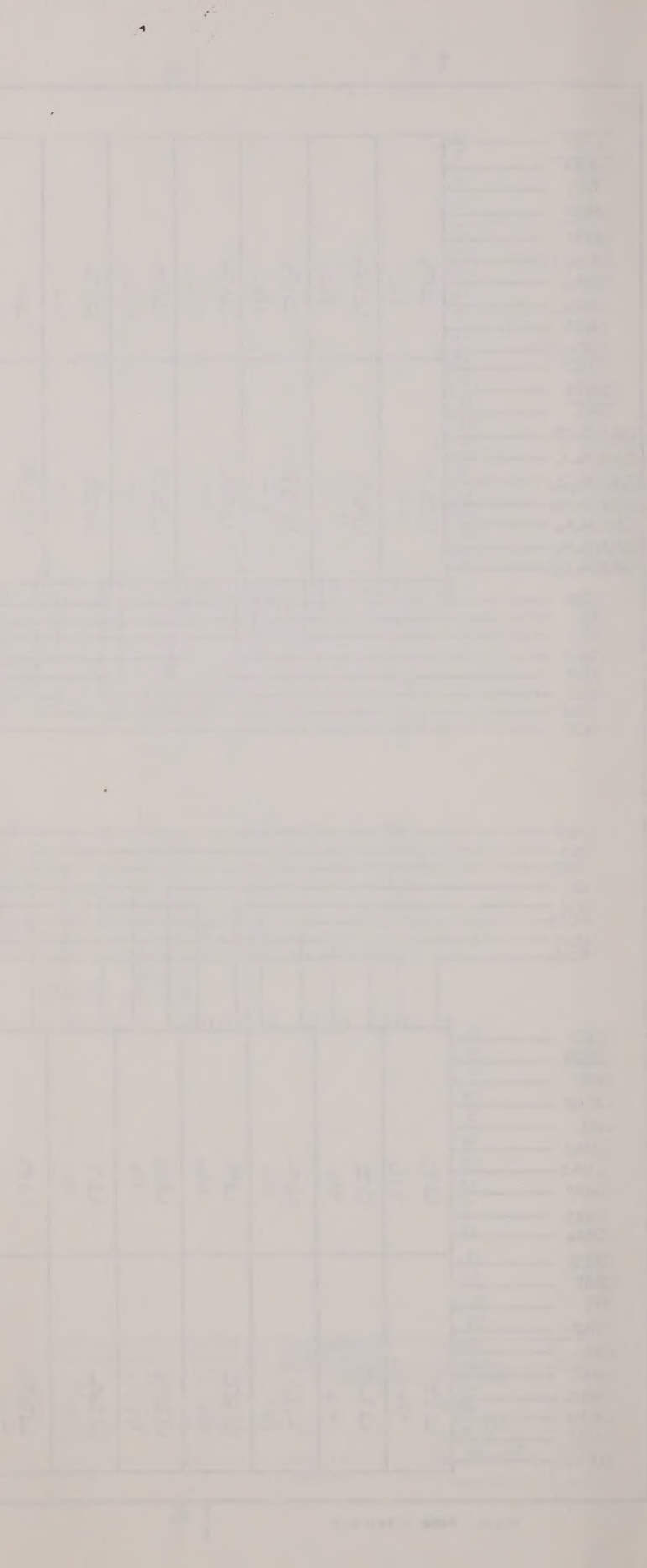
SIZE: C SCALE: NONE

UNIT NO. PS016-001

Model No. V-500

Next Assy.

SHEET 9 OF 9



VISUAL TECHNOLOGY INCORPORATED

540 MAIN STREET, TEWKSBURY, MA 01876, TELEPHONE (617) 851-5000, TELEX 951-539

MAINTENANCE MANUAL/**VISUAL 500/550**

MM500-001-0A
January 1983